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# Design, construction and testing of a reduced-scale cascaded multi-level converter

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# NAVAL POSTGRADUATE SCHOOL
## Monterey, California


# THESIS

**DESIGN, CONSTRUCTION AND TESTING OF A REDUCED-SCALE CASCADED MULTI-LEVEL CONVERTER**

by

Robert A. Crowe

June 2003

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**DESIGN, CONSTRUCTION AND TESTING OF A REDUCED-SCALE CASCADED MULTI-LEVEL CONVERTER**

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Submitted in partial fulfillment of the
requirements for the degree of

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## ABSTRACT

The main focus in the design of the next generation combatant, DD(X), is the US Navy's proposed Integrated Power System (IPS) which includes an all-electric propulsion drive system. The reduction of current waveform harmonics is critical in combatant propulsion systems such as the IPS. One method of reducing the current harmonics is to utilize a multi-level converter topology. The multi-level converter, as compared to a standard converter, features low *dv/dt* losses and low switching losses. This thesis examined the design, construction and testing of two multi-level converters operated in tandem, called a Cascaded Multi-Level Converter (CMLC). A digital logic switching circuit was designed and constructed to control the CMLC during the operational testing phase. The CMLC was demonstrated in a three-phase high-voltage configuration with 178.5 volts zero-to-peak voltage and 2.10 A zero-to-peak current achieved using an R-L load.

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## EXECUTIVE SUMMARY

The U.S. Navy is investing in the development of a ship power generation and utilization architecture that builds on experience in the commercial marine market and adapts commercial technology to the military combatant ship application. This architecture is the backbone of the U.S. Navy's Integrated Power System (IPS) program and it is to be implemented in the next generation of combatants designated the DD(X) family of ships. The major aspect of this IPS is the proposed all-electric propulsion drive where a large portion of the total electric power generated is converted into an appropriate form that can effectively drive large propulsion induction motors.

Reduction of current waveform harmonics is critical in propulsion systems such as IPS. An all-electric ship's acoustic signature is related to shaft torque which in turn is related to motor current harmonics. Although all-electric propulsion drives are mature systems in the commercial marine industry, commercial converters do not produce the desired waveform fidelity that is crucial in a military architecture. Current waveform harmonics can be reduced by controlling a converter with pulse-width modulation (PWM) but at high power, PWM switching frequencies are limited to about 1.5 – 2 kHz since higher frequencies produce sharp waveform edges that create EMI and motor insulation issues. Another method of reducing current harmonics is to utilize a multi-level converter topology; a concept whereby the converter topology allows additional motor phase voltage levels than with a conventional converter. The purpose of this thesis was to document the design, fabrication and testing of a Cascaded Multi-Level Converter (CMLC).

The CMLC is a circuit comprised of inter-connected power transistors and diodes as shown in Figure E-1. By sequentially changing the level of the circuits DC input voltage, the converter produces a quasi-desired AC sinusoidal waveform. The CMLC consists of the following sub-sections/stages: input DC Link voltage, power unit modules, power diodes, and switching circuitry. The power unit module, shown in Figure E-2, consists of the following components: a gate driver circuit board, a power

transistor (IGBT) with accompanying snubber circuit card and heat sink material. The gate driver circuit board provides an 'on' or 'off' gating signal to the IGBT as prescribed by the digital logic switching circuitry.

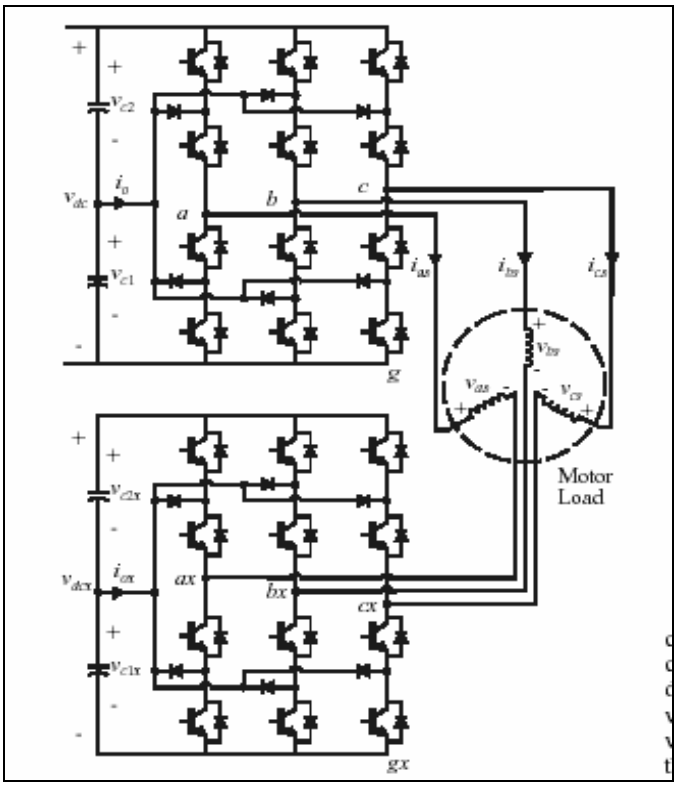


**Figure E-1: The Cascaded Multi-Level Converter [From Ref. 3.]**

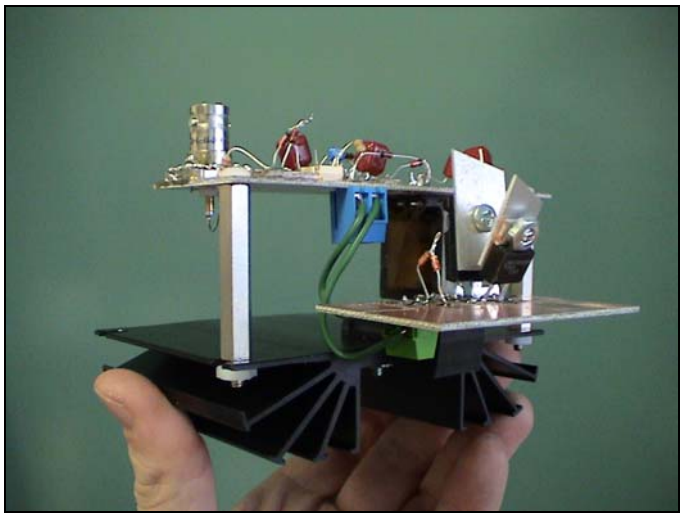

**Figure E-2: The Power Unit Module**

The design of the CMLC sections was initiated by a selection of components based on the converter specifications shown in Table E-1:

**Table E-1: CMLC Specifications**

| Specification | Value |
|---|---|
| Input Power | 240 V / 10 A |
| Input Capacitance | Rated 300 V or greater |
| Transistor Voltage (Blocking) | 1200 V |
| Transistor Current (Collector-to-emitter) | 25 A |
| System Cooling | Finned Type Heat Sinks |

The construction of the gate driver circuit card, IGBT snubber circuit card, and the power supply operational amplifier (power input to the gate driver circuit card) were carried out by populating copper-cladded insulation board with the pre-selected components. Post-construction tests were conducted on the power supply operational amplifier and each power unit module prior to the construction of each converter phase.

Alternate transistor switching techniques are presented in this thesis: the sine-triangle pulse width modulation and space vector modulation. A digital logic switching circuit was ultimately implemented to ensure easier troubleshooting of the converter hardware during testing. Advanced Boolean Expression Language (ABEL) software was used in the programming of the digital logic circuit devices or programmable logic devices (PLDs). A thorough test of the resultant circuit verified switching signals capable of producing a balanced set of three-phase voltages.

Detailed testing of the CMLC was conducted in the NPS power laboratory. Each CMLC phase was tested at low voltage/low current (40 V zero-to-peak and 0.5 A zero-to-peak) conditions to ensure for proper operation and then a two-phase test was conducted to ensure the digital logic circuit produced properly phased output waveforms. Figure E-3 shows the circuit configuration during the low-voltage testing phase. A final high voltage/high current (200 V zero-to-peak and 2.2 A zero-to-peak) test was then

conducted. Figure E-4 is a digital image of the three-phase current output. This testing revealed the CMLC operational results were in agreement with expected values.

This research documented the design, construction and testing a CMLC. Possible areas for future CMLC research include analysis of propulsion shaft noise and analysis/implementation of various switching techniques. Continued research in this dc-ac converter is vital for the future of the U.S. Navy's next breed of combatant ship because CMLC technology offers high power conversion with reduced or eliminated current waveform harmonics.

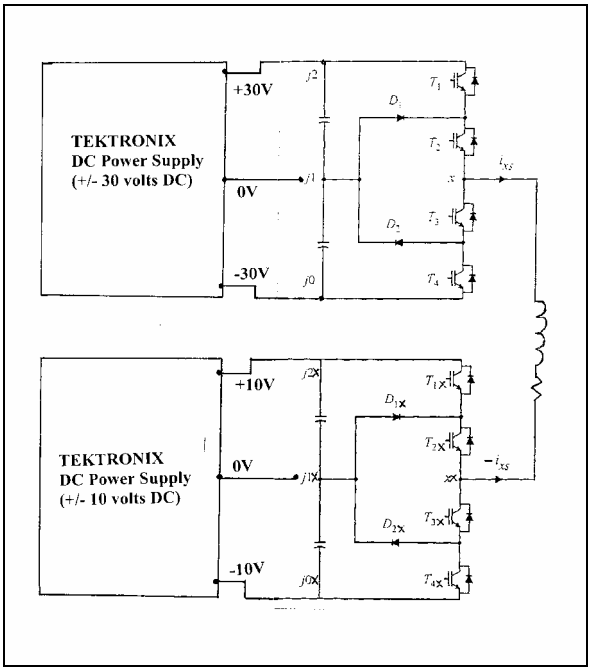


**Figure E-3: Testing Configuration (Low Voltage/Low Current Condition) [From Ref. 6.]**

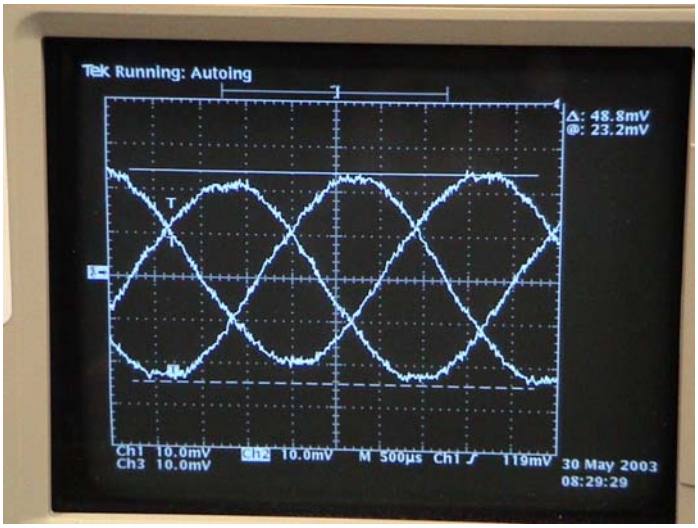


**Figure E-4: Three Phase Current Output with Current Probe @ 1.0 A/DIV**

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# I. INTRODUCTION

## A. POWER REQUIREMENTS FOR NEXT GENERATION SHIP

With the dissolution of the Soviet Union and the emergence of the war on terrorism, the Department of Defense is challenged to both scale back expenditures and produce "transformative" technologies. It has never been more important to develop ships and systems that are cost effective, operationally robust and minimally manned. Presently, U.S. Navy ships are configured with a varied array of mechanical and electrical systems which are independent in nature and in some cases create unnecessary redundancy that degrades fuel efficiency. For example, the Navy's conventional propulsion drive train transfers energy to the drive shafts via a reduction gear; at no time during operation is this prime mover "propulsion" energy made available for other ship systems. Both fuel efficiency and manpower requirements represent major factors in the Total Operating Cost (TOC) of naval ships and systems. In order to cut back total operating costs, U.S. Navy ship design must dramatically move beyond conservative constraints.

One major change in ship design surrounds the electrical power system; the U.S. Navy is targeting an all-electric ship where all major systems including propulsion, aircraft launching and futuristic weapons would be electrically powered [1]. The Navy is calling such an arrangement the Integrated Power System (IPS). Figure 1-1 is a diagram of the representative system showing a prime mover and generator set providing power to a propulsion motor unit as well a providing power to ship service loads via a power conversion module. The IPS would effectively unlock the substantial mechanical power originally dedicated only to propulsion and distribute it to other large power consumers as necessary.

The new architecture for this IPS builds on commercial ship technology that has been in place for many years. The robust and mature commercial marine systems have realized significant fuel savings for the shipping industry throughout the world by more efficiently loading prime mover engines. The motivation to proceed with this IPS design has many factors: it will reduce the number of prime movers, produce fuel savings,

reduce maintenance, allow a reduction in manning and offer a platform that will support new technology weapons.

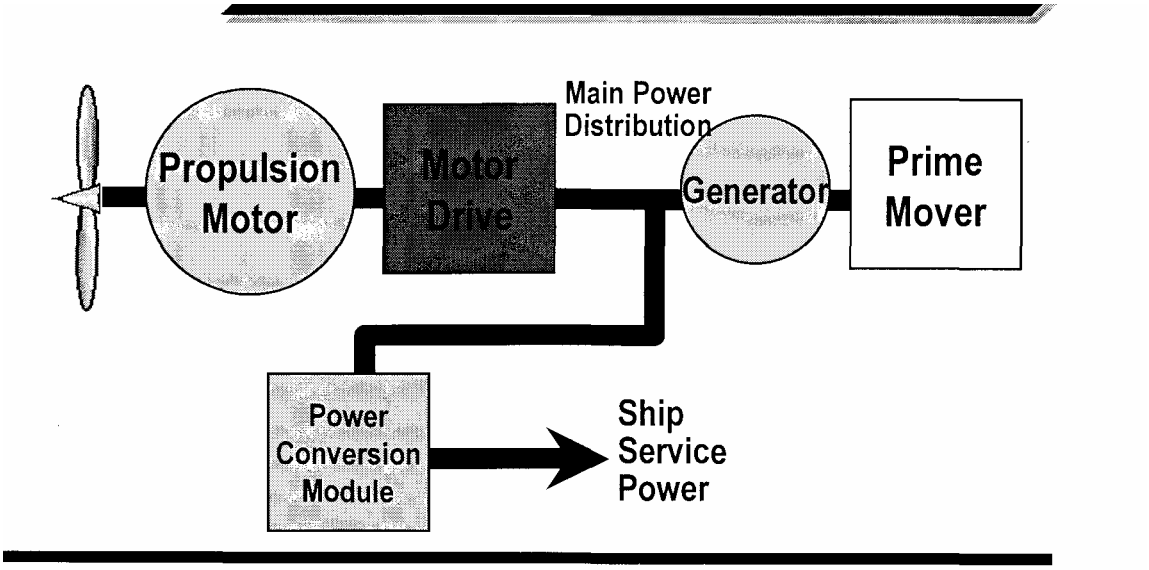



**Figure 1-1: General Concept of the Integrated Power System [From Ref. 1.]**

The IPS must produce higher amounts of power to support all loads including future demands. This need for higher installed power taxes the capability of current energy conversion and power delivery systems. Although high-power systems are common in the commercial ship fleet, military requirements make the research and design efforts more complex. Low electrical signatures, non-interference and damage tolerances are key factors that must be addressed to make this all-electric concept feasible for use in a military architecture. Specifically, in the propulsion drive portion of IPS, the challenge is tapping large amounts of electrical power from a mechanical power source and converting that power into the appropriate waveforms that will run an electric propulsion motor. The key power conversion issue is the reduction or elimination of current-waveform harmonics and, thus, torque harmonics. Current-waveform harmonics at high power levels create noise exceeding military acoustic requirements and necessitate inverter de-rating, implying a larger and heavier propulsion unit [1].

## B. OVERVIEW OF CURRENT RESEARCH FOR ALL ELECTRIC SHIP

This section offers an overview of some of the research currently underway to support the realization of IPS in U.S. Navy ships. Research for the IPS is being fueled by the push to move the Navy's DD(X) program (the future navy warship) from chalkboard or view-graph to the actual cutting of steel or the forming of composite materials in the shipyard. The Navy formed two teams consisting of major shipbuilders and weapon system contractors and had them compete for the design of the proposed DD(X) family of ships. This method of procurement represents a major change in the way the government purchases systems. Through competition, they endeavor to achieve an optimal product while saving design, engineering and research overhead costs.

With a major shipbuilding program of this magnitude and scope underway, there is much research in progress that supports future systems. In the area of weapon systems, the all-electric rail gun and directed energy weapons are high priority systems. In the area of power distribution, the Navy is actively investigating the implementation of a hybrid ac and dc zonal distribution system. No matter what the ship service load is or how it is distributed, the IPS architecture must include a high efficiency dc-ac converter and a compact yet powerful propulsion motor.

A large portion of propulsion motor and dc-ac converter research is being conducted at the IPS Land Based Engineering Site (LBES), located at NAVSESS Philadelphia, Pennsylvania. Major components for testing include a 21.6 MW generator, a 19 MW propulsion motor and converter and a 2 MW ship service distribution system [2]. The prime contractor, Lockheed Martin Ocean Radar and Sensors Division, Syracuse, NY, is handling integration and development of the supervisory control system. Another team, headed up by Dr. Keith Corzine of the University of Wisconsin, built and are currently testing a small proto-type 30-kW multi-level converter. It is in this latter area of research and testing that this thesis research effort is focused.

## C. THE MULTI-LEVEL CONVERTER VS. THE CASCADED MULTI-LEVEL CONVERTER

Figure 1-2 shows a standard diode-clamped multi-level converter consisting of a DC-link voltage ($v_{dc}$) and capacitors as input for the three-phase bank of power transistors which, when sequentially gated 'on' and 'off,' convert the input voltage into an ac-signal for the three-phase inductive load [3]. The use of a multi-level converter is one method of reducing current waveform harmonics at high power. The multi-level converter produces more phase voltage levels than a standard dc-ac converter drive. It is the increased number of output voltage levels that leads to improved harmonic content in the converter waveforms. This increase in voltage levels is achieved with a much lower semiconductor device switching frequency; therefore there are lower switching losses. Multi-level converters produce lower voltage transients (*dv/dt*) which greatly reduces common-mode currents and stresses on motor insulation.

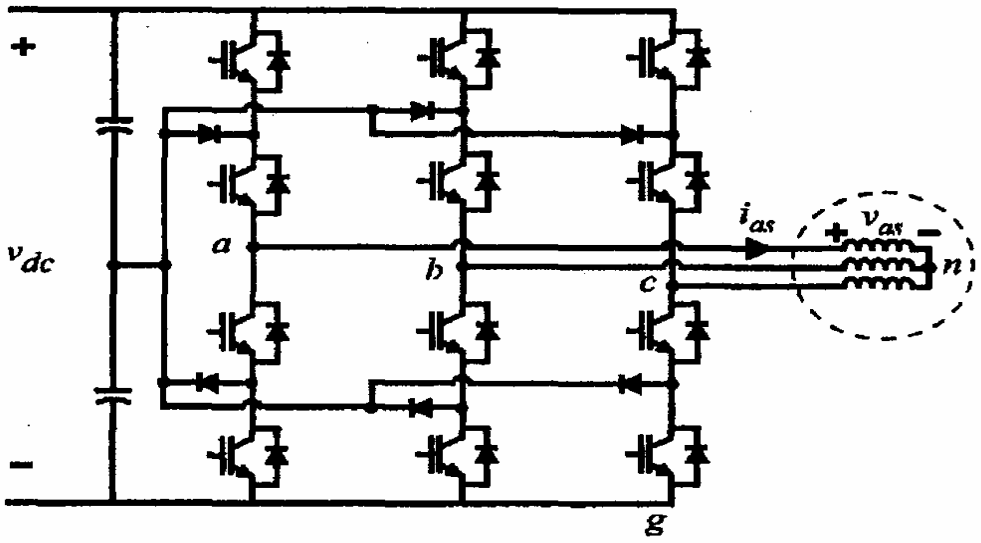



**Figure 1-2: Three-level Multi-Level Converter [From Ref. 3.]**

Multi-level power conversion has become popular due to the advantages described above; however, the primary disadvantage of a multi-level converter is the large number of semiconductor devices that are required in its construction. Semiconductors themselves are not overly expensive. It is the gate-driver circuits that

operate each transistor that are expensive and make the mechanical layout more elaborate.

A new type of multi-level converter (MLC), the cascaded multilevel converter, has been proposed which is constructed from two multi-level converters [4]. The main advantage of the cascaded converter over the standard multi-level converter is that it offers more non-redundant switching states per number of active semiconductor devices, thereby improving converter performance and decreasing converter costs. A cascaded MLC is illustrated in Figure 1-3 [4]. In this figure, two dc-voltage sources supply the upper and lower input capacitors. The three-phase motor load ground is split-out and the three leads are connected to the output phase terminals in the lower level creating a wye-to-wye topology.

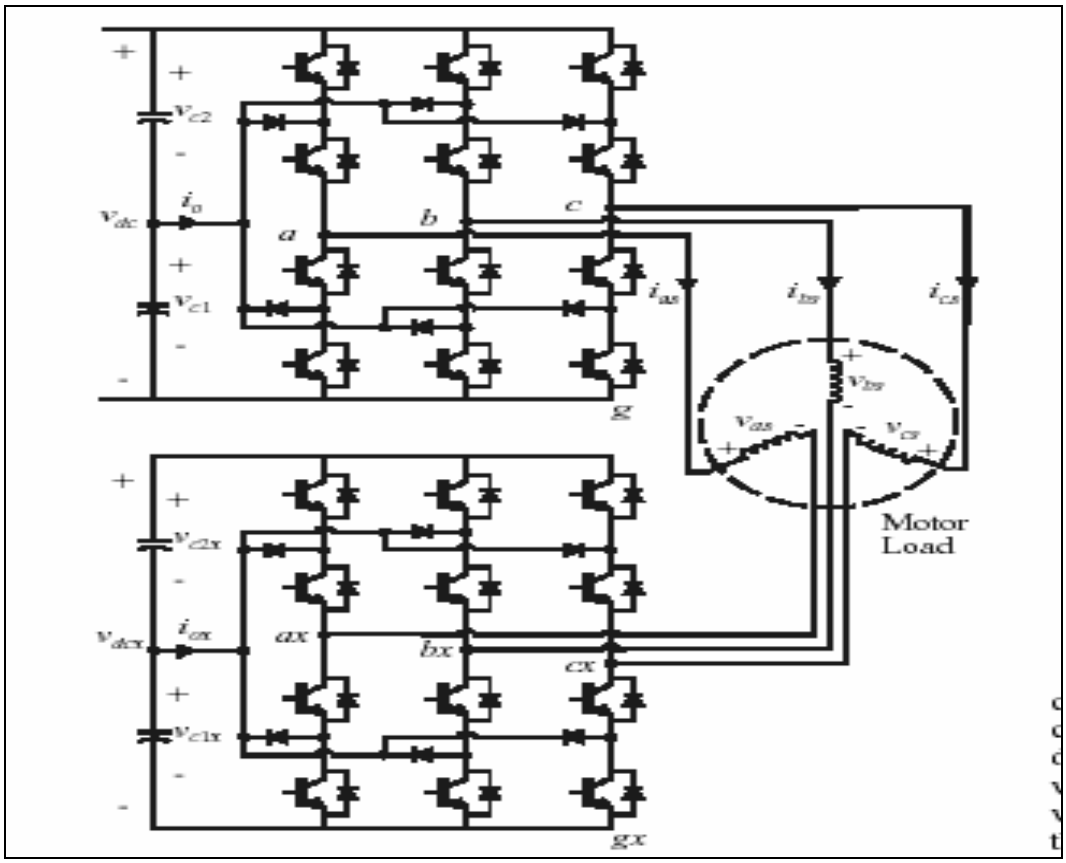



**Figure 1-3: A Cascaded Multi-level Converter [From Ref. 4.]**

## D. THESIS GOAL

The purpose of this thesis research is to thoroughly document the design, development and testing of a reduced-scale prototype cascaded multi-level converter (CMLC). Multi-level conversion is clearly a major research and development component in the Navy's quest to implement IPS. Completed work and products from this thesis will augment the technical resources of the NPS Power Systems Laboratory and support future thesis projects directed by NAVSEA 05 resource sponsors.

## E. THESIS OVERVIEW

Chapter II provides a description of the cascaded multi-level converter and it outlines specifications required to select components for the converter. Chapter III is a detailed description of the selection of components. Chapter IV contains an explanation of the design and construction of the converter. The design and construction of the converter's digital logic controller section is described in Chapter V. Chapter VI documents the testing of the cascaded multi-level converter and Chapter VII provides thesis recommendations and conclusions. The last section consists of appendices containing information that supports the technical discussion presented in the chapters.

# II. CONVERTER DESCRIPTION AND SPECIFICATIONS

## A. PURPOSE

This chapter provides a description of the Cascaded Multi-Level Converter (CMLC) that is reported on in this thesis. Also, this chapter includes a discussion of the specifications for the equipment and systems that are used in the design, development and operation of the CMLC.

## B. DESCRIPTION OF CMLC

In this sub-section, a description of the CMLC is provided. The purpose of the converter is to process a DC voltage signal into an AC voltage signal. Figure 2-1 shows a general overview of the process as required shipboard. As shown, a source generator produces an AC voltage signal. This signal is then rectified by an ac-dc voltage conversion module resulting in a DC-link voltage. The CMLC Switching Transistor section, controlled by switching logic/driver circuit components, takes the DC-link voltage and produces a multi-phase AC signal to be utilized to power a multi-phase AC load.

**Figure 2-1: Overview of DC-AC Conversion Process**

The CMLC switching transistor network, switching logic and driver circuit modules comprise the emphasis of this thesis research. Figure 2-2 shows one leg of a three-phase CMLC. It is a network made up of an upper and lower bank of transistors ($T_1$ thru $T_4$ and $T_{1X}$ thru $T_{4X}$). The banks are connected to the load at points 'x' and 'xx.'

Current may flow from the top rail, through the load, and return via the negative rail of $V_{dc2}$, or it may flow from the top rail of $V_{dc2,}$ through the load and return via the negative rail of $V_{dc1.}$

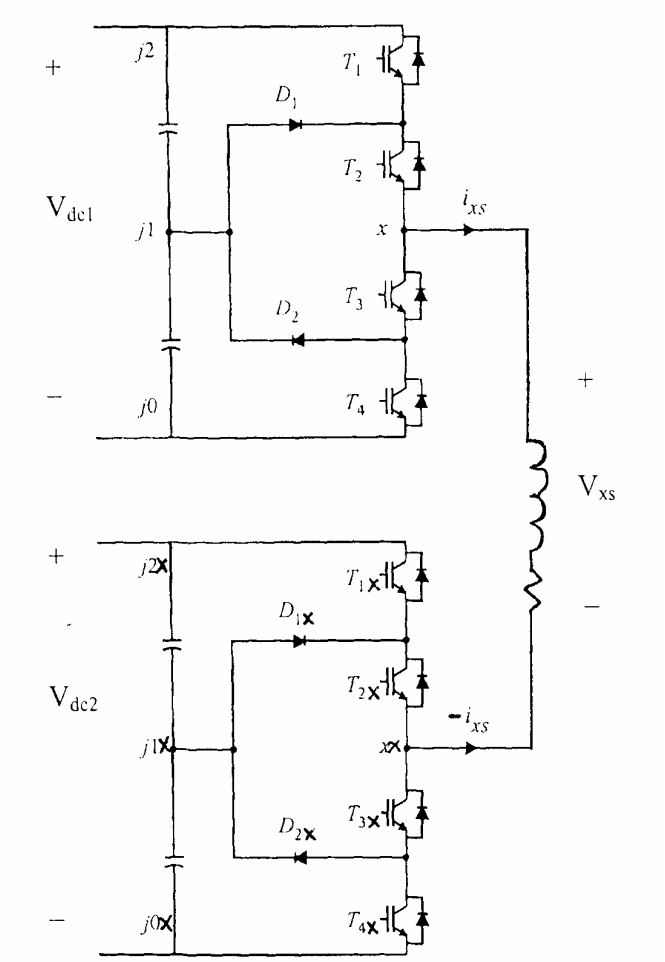



**Figure 2-2: One Leg of the CMLC [From Ref. 3.]**

The CMLC also consists of input capacitors and diodes necessary to realize the additional output voltage levels, labeled $D_1$, $D_2$, $D_{1X}$ and $D_{2X}$. The input capacitors effectively divide the DC link voltages between nodes j0 and j2 and j0x and j2x into $V_{dc1}$ and $V_{dc2}$, respectively. With this DC-link voltage division, the voltage level at each upper and lower portion of the converter can be switched to either 0 volts, to one-half the DC-

link voltage or to the full DC-link voltage level. Since the output voltage level is dictated by

$$v_{xs} = v_x - v_{xx}, \tag{2.1}$$

the CMLC can create nine different voltage combinations as will be shown. As the CMLC is switched between each voltage level, the diodes ($D_1$, $D_2$, $D_{1X}$ and $D_{2X}$) are biased 'off' and 'on' in a manner that connects the appropriate voltage level to the output leg.

The CMLC topology adds flexibility to the design for the operator. By varying the DC-link voltage levels to the upper and lower levels of the converter, different voltage levels can be achieved. The maximum amount of voltage levels, for any given CMLC, is achieved by making the lower dc voltage ($v_{dc2}$) a certain percentage of the upper dc voltage ($v_{dc1}$). This 'maximum voltage level' percentage is determined by using [4]

$$\frac{v_{dc2}}{v_{dc1}} = \frac{n_2 - 1}{n_2 n_1 - n_2}, \tag{2.2}$$

where $n_1$ is the number of levels for the upper converter while $n_2$ is the number of levels for the lower converter. The converter in Figure 2-2 combines two three-level converters, thus the 'maximum voltage level' percentage is

$$\frac{v_{dc2}}{v_{dc1}} = \frac{3-1}{(3)(3)-3} = \frac{1}{3}.$$

For any given CMLC, the maximum amount of voltage levels is determined by [4]

$$nl(\max) = (n_1)(n_2), \tag{2.3}$$

thus, the maximum number of voltage levels that can be obtained by the CMLC in Figure 2-2 is

$$nl(\max) = (3)(3) = 9.$$

Table 2.1 illustrates the different voltage levels that can be achieved with the CMLC. *Sx* and *Sxx* represent the transistor states for each converter. For example, *Sx* = 1 implies that $T_2$ and $T_3$ (Figure 2-2) have been gated whereas *Sxx* = 2 means that $T_{1x}$ and $T_{2x}$ have been gated. The term 'E' is the basic voltage level for the converter; more

specifically it is the voltage across one input capacitor of the lower converter. *Vx* is the upper converter voltage level and *Vxx* is the lower converter voltage level. *Vxs* is the output voltage. Table 2.1 represents the condition where $V_{dc1} = 3V_{dc2}$ and $V_{dc2} = 2\text{E}$.

To obtain an ac sine-wave as an output, the transistors on each level of the converter must be gated in a sequential manner. The gating of each transistor must be carried out using a gate-driver circuit, which in turn is controlled by a switching logic algorithm. The gate driver and the switching logic method are two critical and complex parts of the overall CMLC system. Figure 2-3 is a block diagram that gives an overview of the key elements of the converter design. It is this system that will be emphasized in the ensuing chapters.

| ***Sx*** | ***Sxx*** | ***Vx*** | ***Vxx*** | ***Vxs*** | ***Sxs*** |
|---|---|---|---|---|---|
| 0 | 2 | –3E | 1E | –4E | 0 |
| 0 | 1 | –3E | 0E | –3E | 1 |
| 0 | 0 | –3E | –1E | –2E | 2 |
| 1 | 2 | 0E | 1E | –1E | 3 |
| 1 | 1 | 0E | 0E | 0E | 4 |
| 1 | 0 | 0E | –1E | 1E | 5 |
| 2 | 2 | 3E | 1E | 2E | 6 |
| 2 | 1 | 3E | 0E | 3E | 7 |
| 2 | 0 | 3E | –1E | 4E | 8 |

**Table 2.1: CMLC Voltage Levels**

Before specific components and systems can be identified to document the design and construction of each section depicted in Figure 2-3, a thorough description of the CMLC system specifications must be established. Figure 2-3 is an overview of the CMLC. A DC-link voltage is generated and then placed across the input terminals of the converter. The input terminals consist of input capacitors and voltage-level diodes which

allow the converter to effectively divide the input DC voltage and develop various voltage levels. A switching logic section controls a gate-driver circuit which controls the power transistors thus allowing the input DC voltage be shaped into the desired AC waveform that is supplied to the load.

**Figure 2-3: Overview of the CMLC System**

## C. SPECIFICATIONS

The following subsections describe the key specifications for the CMLC: input power, input capacitance, power transistor voltages and current capacities0, power transistor protection, power source for the gate-driver circuit, the system switching frequency and load and system cooling.

### 1. Input Power

There are various methods of rectifying the ac from the generator to obtain the dc necessary for the input to the propulsion converter; once established, this voltage is dubbed the dc-link voltage. The dc-ac CMLC then utilizes the dc-link as an input and provides the load with the necessary phase-shifted variable frequency waveforms. At NPS, a 208 V, 25 A, 3-phase variac, uncontrolled rectifier bridge and 10 mF of filtering

capacitance are used to establish the dc-link for the upper level of the CMLC. The lower level of the CMLC is fed by a single-phase, 115 VAC input voltage, 0-240 VDC output voltage 'Powerstat.'

### 2. Input Capacitance

The CMLC is designed to operate at various switching frequencies while drawing current from the dc-link voltage source. It is crucial to ensure that the input voltage source remains at a consistent voltage level during operation. A bank of series-connected capacitors with sufficient capacitance will ensure that the input voltage level remains constant, as well as dividing the dc-link voltage to the prescribed number of voltage levels. These capacitors are required to be rated at 300 VDC or greater based on the dc-link voltage specification described above.

### 3. Power Transistor Voltage and Current Capacities

The power transistor that is used for the circuit in this thesis research effort is an Insulated Gate Bipolar Transistor (IGBT). An IGBT is a device that combines the features found in a Bipolar Junction Transistor (BJT) and in a Metal-Oxide-Semiconductor Field Effect Transistor (MOSFET). BJTs have lower conduction losses during the 'on' state, especially in devices with larger blocking voltages, but have longer switching times, especially at 'turn-off.' MOSFETs can be turned 'on' and 'off' much faster, but their on-state conduction losses are larger, especially in devices rated for higher blocking voltages [5].

#### *a. Transistor Voltage*

The IGBT is operated in two states: the blocking state and the conduction state. Manufacturers of these power transistors rate the IGBT by the amount of voltage the transistor can 'block' when it is in the blocking state. This voltage is measured across the collector and emitter nodes and it is labeled $V_{ce}$. A review of the IGBTs available revealed transistors with $V_{ce}$ voltages rated at 1200 V in small chip form and in large package types. Therefore, the blocking state voltage requirement was not a restrictive

design or budget factor, instead it is the current rating through the device that determined the frame-size utilized for the converter design.

***b. Transistor Current***

The most critical design specification for the IGBT is the collector-to-emitter current. It is this specification that relates directly to the packaging type and size of the device. Transistors with a low current rating are in chip form while transistors rated for large currents (300 to 600 A) are packaged as large blocks of semiconductor material with large heat sink areas and heavy duty connectors. In the interest of budget, the specification set for the collector-to-emitter current of the device was 25 A.

### 4. Power Transistor Protection

Power semiconductor transistors are subject to the problem of over-voltage during the switching on and switching off of the device. A common solution that mitigates this problem is the installation of resistor-capacitor-diode (RCD) snubber circuit [6]. Transient over-voltages are addressed by diversion of the energy in the stray inductance to the snubber capacitor during turn-off; the snubber circuit does not address static over-voltages. However, it was found through laboratory tests that static over-voltages were minor compared to transient over-voltages. The snubber capacitor size is based on the energy stored in the stray inductance; the snubber resistor is sized by considering the narrowest pulse in the PWM algorithm and the snubber diode must be a fast type with soft recovery.

### 5. System Switching Frequency and Load

The load that the CLMC will drive during operational testing will mimic the steady-state characteristics of an induction motor. In order to achieve this simulation, a large inductor in series with a bank of resistors was utilized. The inductor and the switching frequency determine the impedance of the load as well as govern the phase angle of the output current. The relationships between inductance ($L$) and the switching frequency ($f$) are [7]

$$X = 2\pi fL, \tag{2-4}$$

$$Z = R + jX, \tag{2-5}$$

$$\theta = \tan^{-1}\left(\frac{X}{R}\right), \tag{2-6}$$

and

$$I = \frac{V}{|Z| \angle \theta}. \tag{2-7}$$

### 6. Power Source for the Gate Driver Circuit

A specification for the power source that drives the transistor gate driver circuit is that it must be completely isolated from the rest of the circuit in order to avoid a ground fault during the operation of the converter. A review of the available gate driver circuits with independent power supplies revealed many capable designs; however, the prohibitive costs of each precluded their application in this project.

### 7. System Cooling

The heat generated by each component in the CMLC is dependent on the current that the device is carrying. The specification of 25 A for the transistor collector-to-emitter current allowed the procurement of all circuit devices in chip form. This in turn set the requirement for heat sink material to be the "finned" metal type capable of being affixed to the heat sink area of each device frame.

## D. SUMMARY

This chapter described the purpose and operation of the CMLC. Also, specifications were set for all the systems and components that are used in the design and operation of the CLMC. Identifying the specifications was a crucial step towards the design of the converter and recognizing what components were needed to be procured. The next chapter documents in detail the design considerations and the selection of components for the converter.

# III. COMPONENT SELECTION

## A. PURPOSE

The purpose of this chapter is to document the component selection for the design and building of the CMLC circuit.

## B. COMPONENT SELECTION FOR THE CONVERTER SECTION

The following sub-section describes the component selection of the input-voltage capacitors, the voltage-level diodes, the IGBT and the protective snubber circuit and the resistor-inductor load. Figure 3-1 shows the upper level of the CMLC provided to enhance the description of this component selection.

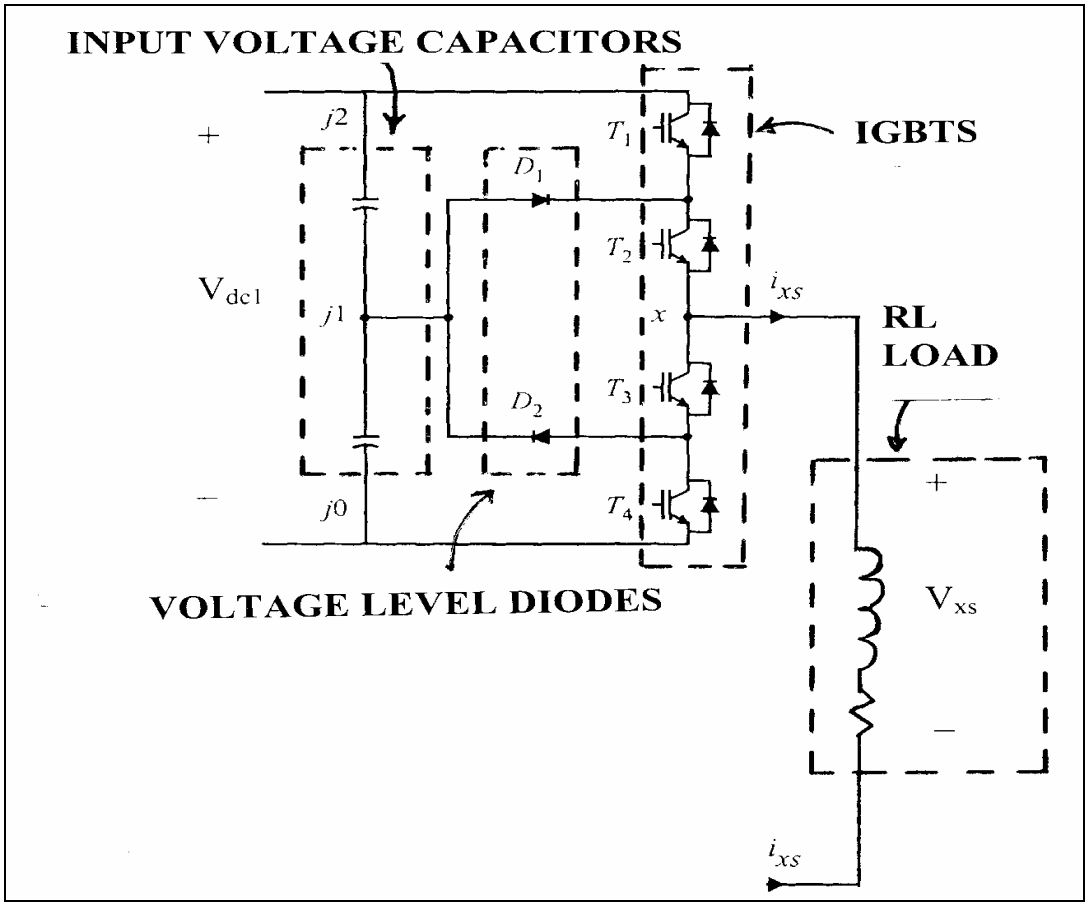



**Figure 3-1: Upper Level of the CMLC**

### 1. Input Voltage Capacitor

As discussed in Chapter II, the input voltage to the converter requires substantial capacitance to divide the dc-link voltage into the prescribed number of voltage levels and to ensure the voltage level remains constant during operation. The capacitor chosen for this role was the Mallory Type-CGH Computer-Grade capacitor. These capacitors are rated at 1000 μF, 450 VDC, and have a high ripple current capability.

### 2. Voltage Level Diodes

High-voltage power diodes are required for the converter to switch instantaneously through its available voltage levels and maintain the proper voltage level prescribed during transistor sequencing. The POWEREX Fast-Recovery Single-Module diode was selected. This device, rated at 50 A of forward current and a maximum reverse voltage of 1200 V, meets the requirements and specifications set in Chapter II. The diode is pictured below in Figure 3-2 and the device's specification sheet is included in Appendix A.

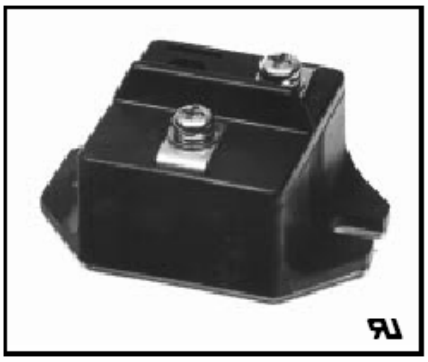


**Figure 3-2: The POWEREX Fast Recovery Diode [From Ref. 13.]**

### 3. IGBT

The selection of the IGBT was mainly budget driven. The relatively low cost International Rectifier IRG4PH50KD IGBT was selected. The IRG4PH50KD IGBT is constructed with an ultra-fast soft recovery diode. The device is rated at $V_{CES}$ = 1200 V and $V_{GE}$ = 15 V. For operation in the on-state, the collector current is rated at 24 A. Most importantly, the IGBT combines low conduction losses with high switching speeds. The

'Turn Off Delay' time is 140 ns and the 'Turn On Delay' time is 67 ns. These ratings fully support the specification limits addressed in Chapter II.

### 4. IGBT Snubber Circuit

As discussed in Chapter II, the IGBT requires protection from transient over-voltages induced by stray inductance. An RCD snubber circuit, Figure (3-3), was designed and built to perform this protective function. The key circuit parameter that is needed for calculating the values of the snubber circuit components is the stray inductance. A typical value of stray inductance is approximately 100 nH [1].

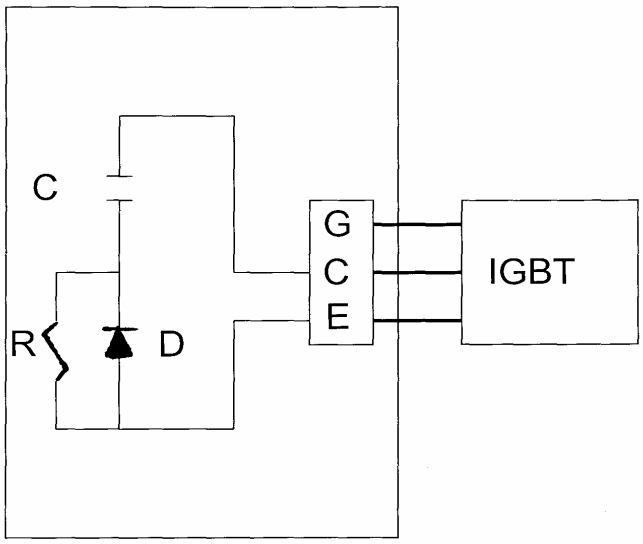



**Figure 3-3: RCD Snubber Circuit**

Equating the energy of the snubber capacitor to the stray inductance and solving for $C$ results in

$$C = L_{stray}\left(\frac{I}{V}\right)^2. \qquad (3\text{-}1)$$

In Equation 3-1, $I$ is the peak current in the IGBT and $V$ is the desired voltage after turn-off. Expected maximum values for $I$ and $V$ are 25 A and 60 V, respectively. With these values, $C = 0.01736$ μF. Therefore a 0.018 μF, 630 V, polypropylene capacitor

was selected as the snubber capacitor. The next step was the calculation of the snubber resistor value. The entering argument for this calculation is the determination of the smallest time value between transistor turn-off and turn-on. A conservative value of $t_{\min} = 1\,\mu s$ was chosen. The equation for the resistor value is

$$R = \frac{t_{\min}}{5C}. \tag{3-2}$$

Using Equation 3-2, the required value of R is 10 Ω [5].

The power requirement for the resistor is found by using [5]

$$P_s = \frac{1}{2} C V^2 f_{sw}. \tag{3-3}$$

At a high switching frequency of 20 kHz, the power rating of the resistor should be 11.2 W or higher. Due to load constraints, the actual switching frequency of the CMLC is approximately 225 Hz. Therefore, the resistor chosen for the circuit, a 10-ohm, 25-watt device is a conservative choice.

The requirement for a fast type with soft recovery diode was fulfilled using the International Rectifier HEXFRED HFA25PB60 ultra-fast, soft recovery diode.

#### 5. Load Resistor/Inductor

The combination resistor and inductor unit for the load is comprised of NPS Power Laboratory components. The lab is equipped with inductors rated at 42.5 mH and 10 A. Also available is a resistor unit rated at 115 V or 230 V with resistance values ranging from 29 ohms to 174 ohms (dependent on voltage source). The switching frequency determines the amount of resistance and inductance used during the testing phase. Also the 10 A rating of the available inductor sets the limit of total current in the circuit, unless other inductors are placed in the load in parallel.

## C. COMPONENT SELECTION FOR THE IGBT GATE DRIVER CIRCUIT

This sub-section describes the selection of components for the gate driver circuit: namely the power supply operational amplifier, the gate driver chip and its supporting circuitry. Figure 3-4 is a diagram provided to enhance the description of this component selection.

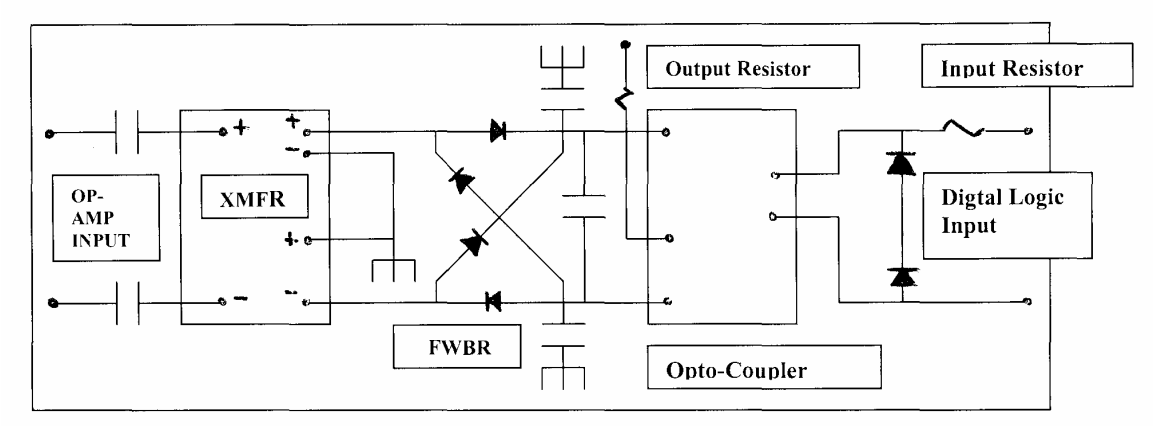



**Figure 3-4: Diagram for Gate Driver Circuit Component Selection**

### 1. Power Supply Op-Amp

The voltage signal needed for the input of each gate driver circuit card requires a waveform generator that can provide an output current of 7.5 A. The NPS Power Laboratory is equipped with a TEXTRONIX CFG-280 function generator that can produce a sine, square or saw-tooth wave at a frequency ranging from 1 Hz to 11 MHz. However, it cannot support a 7.5 A output current. An operational amplifier was required in order to boost this signal and be robust enough to handle the large current draw.

The National Semiconductor LM12CL 80W Operational Amplifier (Op-Amp) was chosen for this purpose. The LM12CL is capable of driving ± 25 V at ± 10 A while operating from a ± 30 V supply. The power bandwidth of the device is 60 kHz. The output from this Op-Amp will provide input into the Gate Driver Circuit card.

### 2. Components for the Gate Driver Circuit Card

#### a. *Transformer*

In order to make each IGBT an independent floating switch (and avoid multiple ground loops), a high frequency (HF) transformer was utilized for galvanic isolation. Each IGBT requires a gate-circuit dc power source that is physically connected to the emitter of the IGBT. Although the source does not need to be highly regulated, it must not exceed the maximum allowable gate voltage (15 V) for the chosen

IGBT. At NPS, a central HF ac source was used to distribute power to the primary side of multiple transformers with very low primary-to-secondary coupling capacitance.

The transformer chosen was the MagneTek SwitchMode/High Frequency Gate Drive Transformer (GDE25-2). It is rated with a turns-ratio of 1:1, a maximum leakage of 2.5 μH and a minimum inductance of 0.68 mH. The technical sheet for this single- input, double-output transformer is included in Appendix A.

**b.** ***Decoupling Capacitor***

In order to eliminate the DC signal from the input to the transformer, a decoupling capacitor is required. The Panasonic 1.0 μF, 50-volt, Stacked Metallized-Film capacitor was chosen for this purpose.

**c.** ***Full Wave Bridge Rectifier***

The rectification of the transformer AC output signal to positive and negative DC voltage levels was achieved with the use of a full-wave-bridge-rectifier (FWBR) configuration. The 1N4148 Rectifier Diode was selected for use in the design of the FWBR. It is a 500 mW, 100-volt, silicon-epitaxial diode with a reverse recovery time of 4 ns.

**d.** ***Opto-coupled Gate Driver Chip***

The TOSHIBA TLP-250 was selected for the gate driving circuit for the International Rectifier IGBT. This device consists of a Gallium-Aluminum-Arsenide light emitting diode and an integrated photo-detector. It is an 8-pin device and a diagram of component is shown below in Figure 3-5. Its recommended operating conditions include an input current of 8 mA and a supply voltage of ± 15 V.

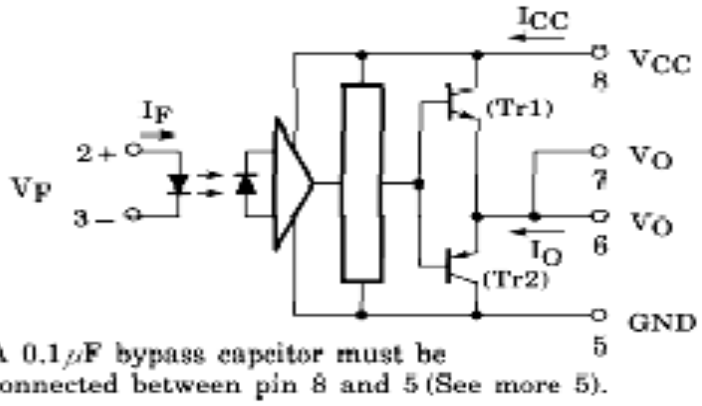



**Figure 3-5: Schematic of Opto-Coupled Gate Driver Chip [From Ref. 11.]**

1. Gate Driver Capacitor. A requirement for the input side of the gate driver chip is the placement of a 1.0 μF capacitor across the positive and negative voltage input leads. The Panasonic 1.0 μF, 50-volt, Ceramic Multi-layer, Radial-Leaded capacitor was chosen for this function.

2. Gate Driver Chip Output Resistor. The current rating from the output of the gate driver to the gate of the transistor is ± 0.5 amps. A 5-ohm resistor is required to achieve this current rating.

3. Gate Driver Chip Input Resistor. The input signal to the gate driver chip should operate at 10 mA. With a 5-volt input signal coming from the logic section, and a 1.6 -volt rating across the input diode of the driver, a 360-ohm resistor is required to obtain the 10 mA current into the device.

## D. SUMMARY

This chapter focused on the selection of components required for the design and development of the converter and for the gate driver circuit needed to drive the converter's IGBT network. The following chapter provides a description of the converter, gate driver and op-amp power supply circuits that were designed and built for operation.

# IV. DESIGN/CONSTRUCTION OF CONVERTER POWER UNIT AND CASCADED MULTI-LEVEL CONVERTER

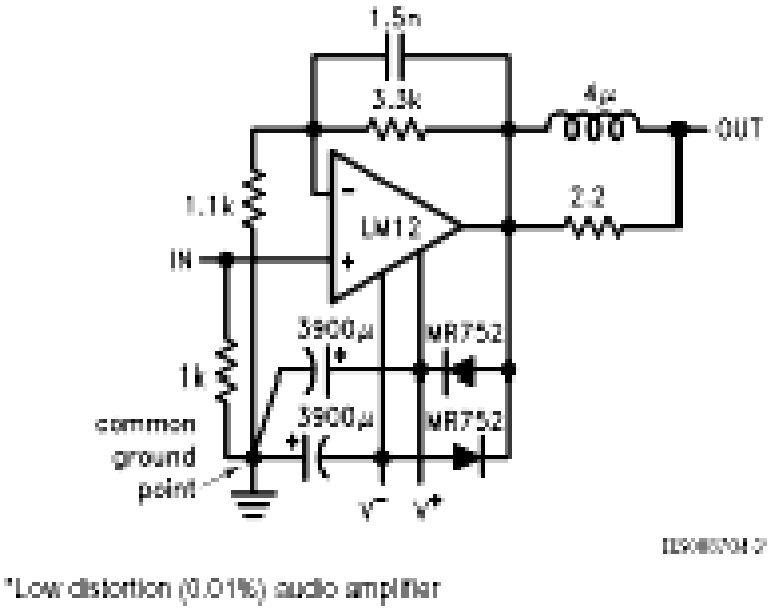
## A. PURPOSE

This chapter contains a description of the design and construction process of the Cascaded Multi-Level Converter (CMLC). The overall CMLC design consists of twenty-four inter-connected, individual 'power' units. A power unit is a standardized module that includes an IGBT and heat sink platform with a snubber circuit card and a gate-driver circuit card. The following sub-sections describe, in detail, the power supply op-amp, each section of this power unit and the design and construction of the CMLC.

## B. DESIGN OF THE POWER SUPPLY OPERATIONAL AMPLIFIER

Each gate-driver power circuit in the converter circuit requires a 30-volt, 20 kHz input sine wave. The TEXTRONIX 11 MHz Function Generator, available in the NPS Power Laboratory, has a maximum output of 10 V. Therefore, it is not capable of meeting the 30 V requirement, nor is it capable of providing the total current drawn from each gate-driver power circuit.

An operational amplifier circuit is required to amplify the function generator output. The National Semiconductor LM12CL 80W Operational Amplifier was procured to perform this function. Figure 4-1 shows the manufacturer's recommended schematic for the Op-Amp for configuration as an audio amplifier.




"Low distortion (0.01%) audio amplifier

**Figure 4-1: LM12CL Op-Amp Schematic [From Ref. 12.]**

The dc-gain of the audio amplifier is '4' as determined by

$$G_{dc} = 1 + \frac{R_f}{R_1} \approx 1 + \frac{3.3}{1.1} \approx 4 \tag{4-1}$$

This dc-gain is sufficient to achieve the amplification of the function generator output to the 30-volt requirement.

The frequency response of the amplifier design was verified using MATLAB's built-in bode-plot analysis software. Appendix B-1 is the MATLAB Code written for this analysis. The results of the Bode plot, Figure 4-2, obtained from the ac-gain

$$G_{ac} = \frac{\left(R_f\right)\left(R_1\right)\left(C_1\right)s + \left(R_f + R_1\right)}{\left(R_f\right)\left(R_1\right)\left(C_1\right)s + R_1} \tag{4-2}$$

shows the audio amplifier providing sufficient gain throughout the planned operating frequency of 20 kHz. In Equation (4-2), $R_f$ = 3.3 kΩ, $R_1$ = 1.1 kΩ, and $C_1$ = 1.5 nF, thus,

$$G_{ac} = \frac{\left(3.3\times10^{3}\right)\left(1.1\times10^{3}\right)\left(1.5\times10^{-9}\right)s+\left(4.4\times10^{3}\right)}{\left(3.3\times10^{3}\right)\left(1.1\times10^{3}\right)\left(1.5\times10^{-9}\right)s+\left(1.1\times10^{3}\right)} = \frac{\left(5.445\times10^{-3}\right)s+\left(4.4\times10^{3}\right)}{\left(5.445\times10^{-3}\right)s+\left(1.1\times10^{3}\right)}$$

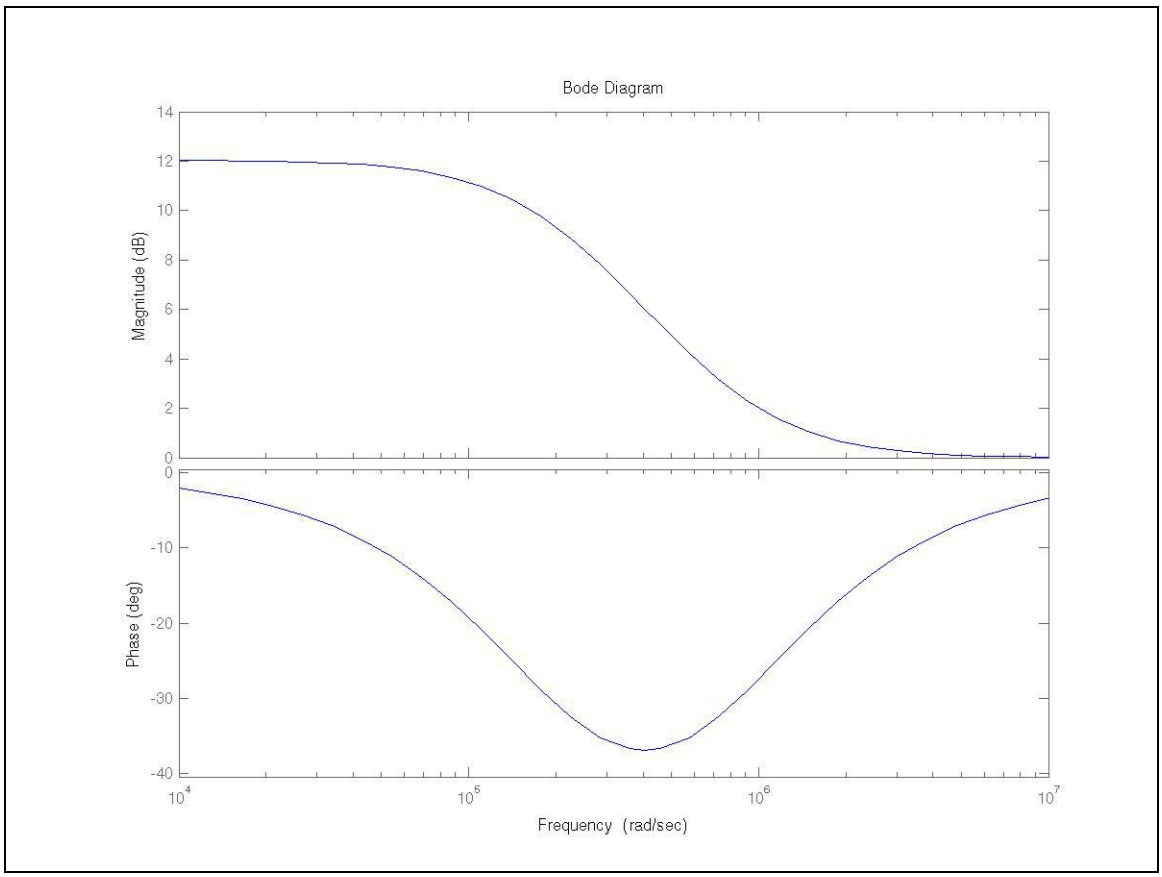



**Figure 4-2: Frequency Response of Op-Amp Circuit**

It was determined that the components recommended by the manufacturer to build the op-amp circuit were sufficient; however, in addition to the schematic, the application of a heat sink for the Op-Amp was determined to be necessary. The use of Wakefield Engineering Type 341K heat sinks properly drilled to allow the op-amp leads to connect to the supporting circuit allows for the effective cooling of the amplifier.

## C. DESIGN OF IGBT GATE DRIVER POWER CIRCUIT

The centerpiece of the gate driver circuit is the opto-coupler gate driver chip. The chip requires ± 15 V of supply voltage and a digital input voltage (0 or 5 V) to produce

the needed output signal to the IGBT gate circuit. The ± 15 V will be obtained by feeding the Power Supply Op-Amp's 30 V, 20 kHz sine-wave through the 1:1 Dual Output Transformer and then through a full wave bridge rectifier.

Figure 4-3 shows the configuration of the transformer and the rectifier diodes that provides an output of ± 15 V. The dual outputs of the transformer are connected in series, making the common connection point the system ground. This allows the positive portion of the 30 V sine-wave to feed into the top half of the FWBR and the negative portion of the sine wave to feed into the bottom half of the FWBR. To ensure any dc offset is eliminated from the input signal, 1.0 μF capacitors were placed in series with the positive and negative input leads of the transformer.

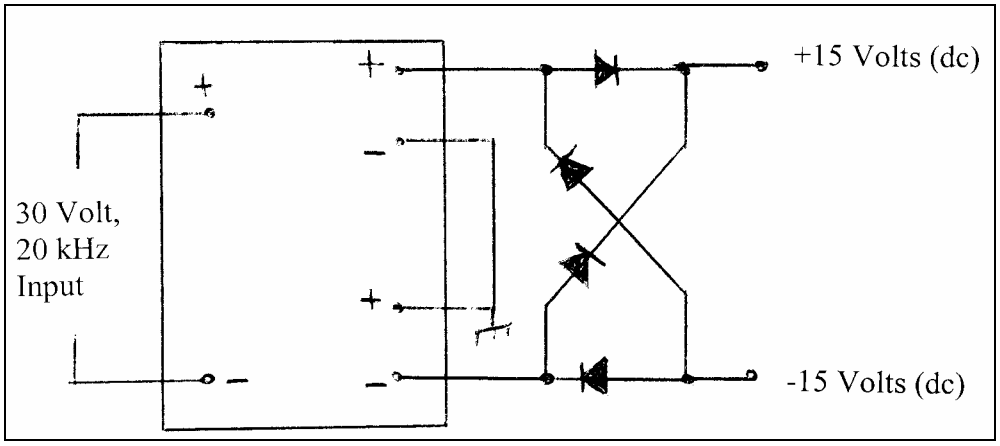



**Figure 4-3: Diagram of Transformer and Full Wave Bridge Rectifier**

Figure 4-4 shows the pin configuration of the opto-coupled gate driver chip or, simply, the opto-coupler. The positive 15 V signal connects to pin 8 and the negative 15 V signal connects to pin 5. The digital signal input is connected across pins 2 and 3. The output signal from the chip, the signal that controls the IGBT gate, connects to the IGBT from pin 7 and through a 5-ohm resistor.

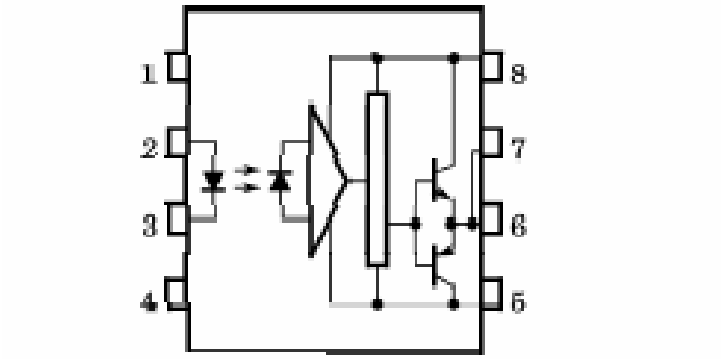



**Figure 4-4: Pin Configuration for Opto-Coupled Gate Driver Chip [From Ref. 12.]**

The digital input signal to the gate driver chip must be isolated from the rest of the gate driver circuit and the converter circuit. More importantly, the input signal voltage must be diode-clamped to match the voltage drop caused by the opto-coupler's input diode. This is accomplished by a series connection of two rectifier diodes placed across the positive and negative leads of the input. To limit the input current into the gate-driver chip to 10 mA, a 360 Ω resistor, was introduced. Figure 4-5 is a sketch of the complete gate-driver circuit including the decoupling capacitors.

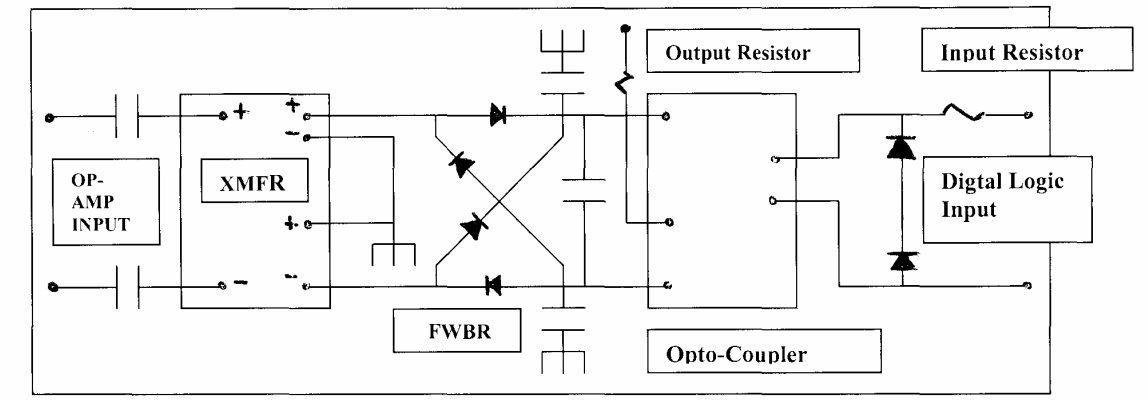



**Figure 4-5: Gate Driver Circuit**

## D. DESIGN OF IGBT/SNUBBER CIRCUIT CARD

The IGBT and the snubber circuit carry a large current during the operation of the converter. An important aspect for the design of the IGBT and snubber circuit tandem is the effective heat removal for the IGBT and the snubber circuit diode and resistor. For this circuit, the IGBT will be mounted flush onto the Wakefield Engineering Type 641K heat sink with the leads pointing out over the edge of the sink. The transistor positioned in this manner, as shown in Figure 4-6, will allow the snubber circuit be connected to the IGBT and away from its heat sink.

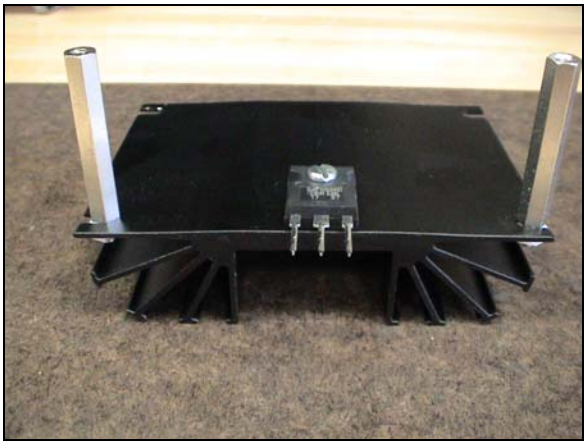


**Figure 4-6: IGBT Mounted to Heat Sink**

Figure 4-7 (previously shown in Chapter III) shows the proper layout of the snubber capacitor, resistor and diode. Not shown is the required protection for the IGBT gate from static discharge. The final design includes a cathode-to-cathode zener diode tandem connecting the gate with the emitter and circuit ground protecting the transistor.

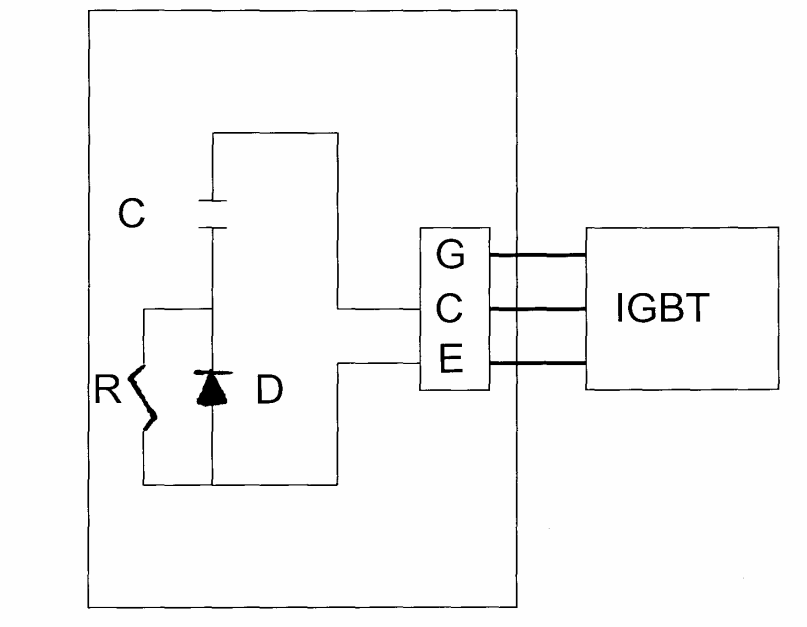



**Figure 4-7: RCD Snubber Circuit**

## E. DISCUSSION OF CIRCUIT CONSTRUCTION MATERIAL

The platform for each circuit board is copper clad insulator material. This material is used in industry for circuit board design and is usually processed using a CAD-CAM system which cuts copper pathways and drills holes for components with precision. In the interest of budget constraints, all circuit boards processed for this thesis work were created with a hand held manual drilling tool. Another technique used to develop copper pathways between nodes was the gluing of copper clad insulator board "strips" to the circuit board surface. This particular technique greatly simplified the building process by minimizing the amount of hand-held drilling required. All components were soldered to the circuit board material using tin alloy solder.

## F. BUILD OF POWER SUPPLY OPERATIONAL AMPLIFIER

The first module built was the Power Supply Operational Amplifier. Figure 4-8 displays the template used to layout the circuit board. The following list is a description of the symbols used for this template and all following circuit templates:

-- Solid lines (including some with hash marks) indicate copper clad strips glued to circuit board.

-- Dotted lines indicate copper pathways formed using hand-held tool.

-- ‘x’ indicates soldering points.

-- ‘o’ indicate drilled holes for components.

**Figure 4-8: Circuit Board for Power Supply Operational Amp**

This circuit board, once constructed, was attached to the op-amp and two heat sinks by soldering the op-amp leads where they passed through the circuit board. Figure 4-9 shows the front view of the built circuit. Figure 4-10 shows the op-amp and the heat sinks.

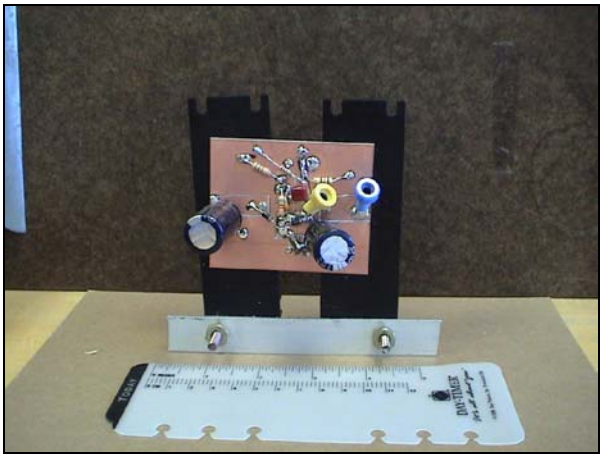


**Figure 4-9: Power Supply Op-Amp Circuit (Front)**

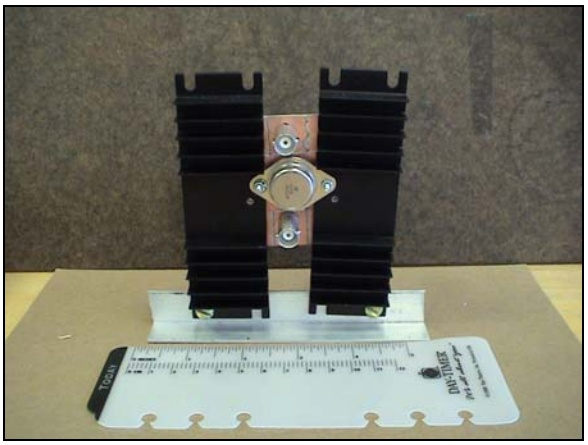


**Figure 4-10: Power Supply Op-Amp Circuit (Back)**

## G. BUILD OF IGBT GATE DRIVER CHIP POWER CIRCUIT

The most complex circuit to build was the gate driver circuit. This was a complex design and build due to the amount of and the size of the parts used for this circuit board. Components used were: 1 transformer, 1 gate-driver chip, 6 rectifier diodes, 5 capacitors, 2 resistors, 4 connectors, and 9 strips of copper clad. The major challenge for this circuit board was the positioning of the transformer and the gate driver chip. The transformer's bulky size (1.5 inches by 1.5 inches) was the reason for the device being mounted to the underside of the circuit board with the leads passing through to the top surface. The gate driver chip was turned up-side down and glued to the circuit board top surface allowing the leads to be exposed for the soldering of the required input leads. Figure 4-11 shows the template used to construct the circuit.

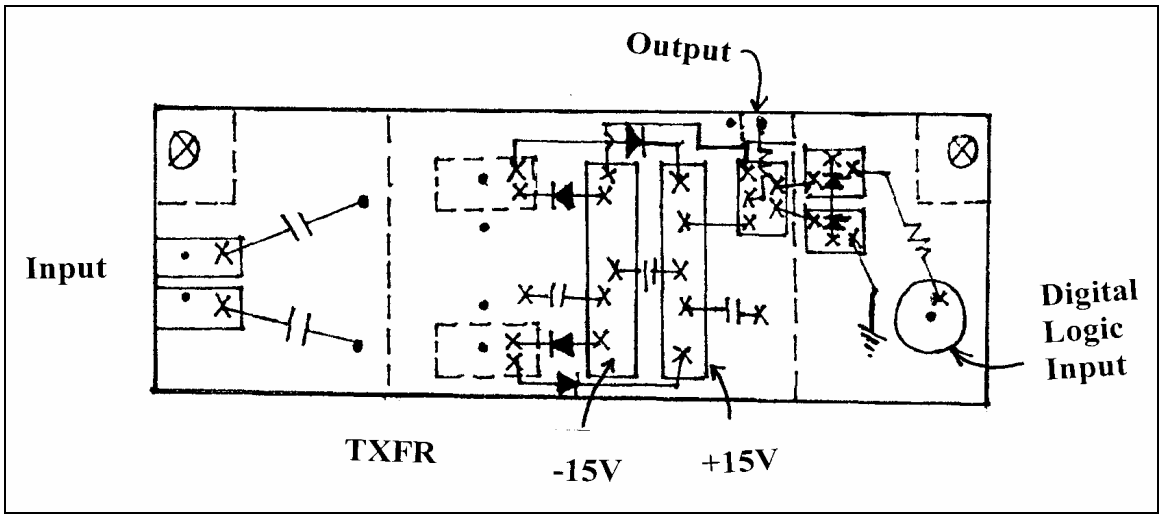



**Figure 4-11: Gate Driver Circuit Board Template**

Figure 4-12 is a digital image of one constructed gate-driver circuit board. Figure 4-13 is the bottom view showing the transformer and the input and output connectors.

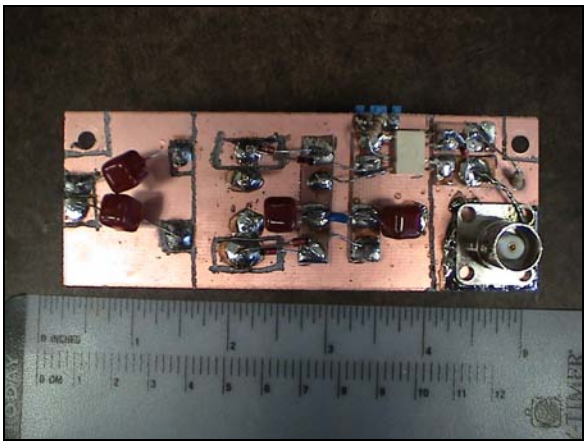


**Figure 4-13: Gate Driver Circuit Board (Top View)**

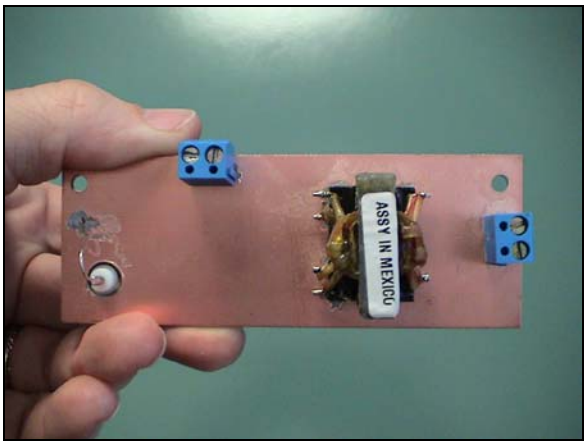



**Figure 4-13: Bottom View of Gate Driver Circuit Board**

In Figure 4-13, the blue connector on the right hand side is the input terminals for the 20 kHz power supply and the top blue connector is where the board connects to the IGBT gate and to system ground.

## H. BUILD OF IGBT SNUBBER CIRCUIT CARD

The construction of the IGBT snubber circuit card involved the soldering of five components. The challenge with this circuit was the placement of the diode, resistor and capacitor. To ensure the snubber circuit operates effectively and in an optimal manner, the distance between the diode, resistor and capacitor leads must be minimized to within a few millimeters. This requirement made the soldering of these components a tedious task. Figure 4-14 is the template used to build the snubber circuit card.

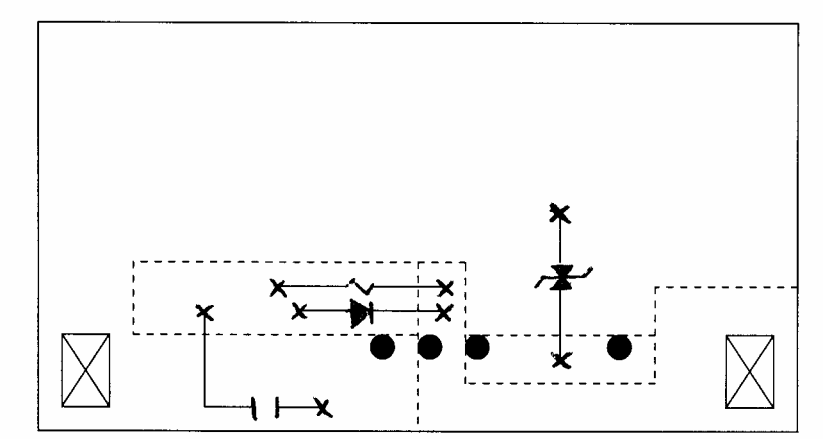


**Figure 4-14: Snubber Circuit Card Template**

Figure 4-15 is a digital image of a completed snubber circuit card. This figure shows the diode and the resistor with their aluminum-strip heat sinks attached. Figure 4-16 is the side view of a completed snubber card. At this angle, the connectors are visible. The black connector is where the IGBT leads connects to the circuit card and the green connector is where the IGBT gate and emitter (ground) connects to the gate driver circuit card.

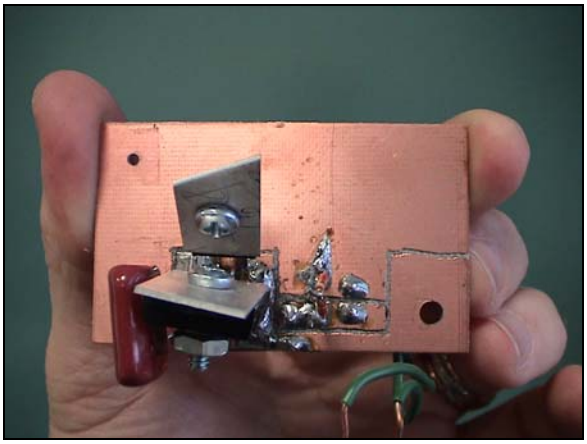


**Figure 4-15: IGBT Snubber Circuit Card (Top View)**

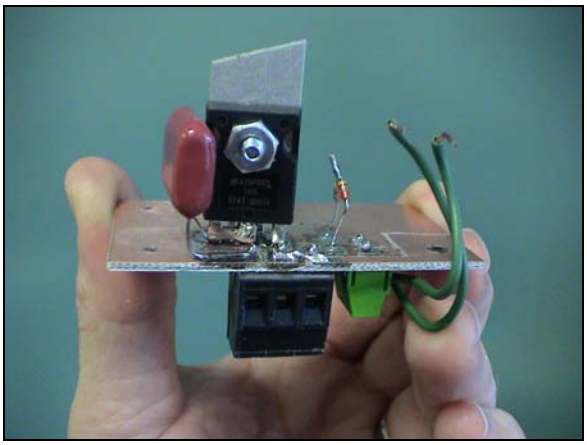


**Figure 4-16: Side View of IGBT Snubber Circuit Card**

## I. THE CMLC POWER UNIT

Each constructed IGBT and heat sink module, gate-driver circuit card and snubber circuit card were assembled to form the CMLC power unit. Figure 4-17 is a digital image depicting the CMLC power unit. The gate-driver circuit card was elevated above the surface of the IGBT heat sink using two metal posts with plastic nuts. This design allowed for the gate-driver circuit card to be far enough away from the heat generated by the IGBT during operation while keeping the length of wire between the card and the IGBT gate as short as possible.

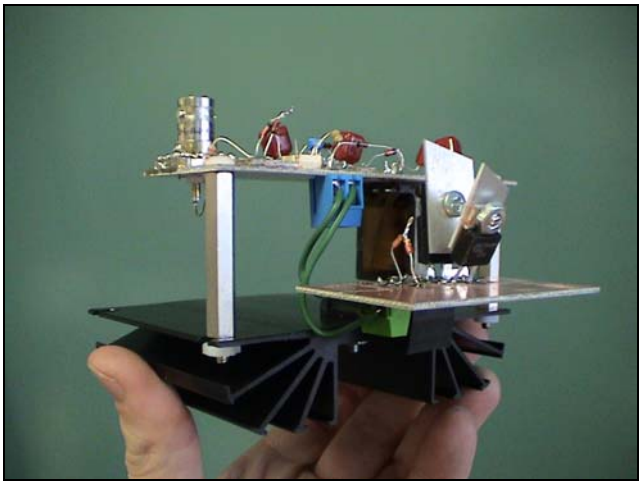


**Figure 4-17: The CMLC Power Unit**

## J. DESIGN/CONSTRUCTION OF CASCADED MULTI-LEVEL CONVERTER (CMLC)

Twenty-four power units were constructed for use in configuring a three-phase cascaded multi-level converter (each phase consisting of eight power units). These power units were connected together, to clamping power diodes, using flat-bar copper pieces cut and drilled and then bolted to pre-drilled holes on the snubber circuit card and on the diodes. The entire phase configuration was then attached to a vertical wooden structure. The circuit configuration was made vertical to allow for easier reconfiguration of power units and troubleshooting of the circuit during testing of the CMLC. Figure 4-18 is digital image showing a completed phase of the CMLC.

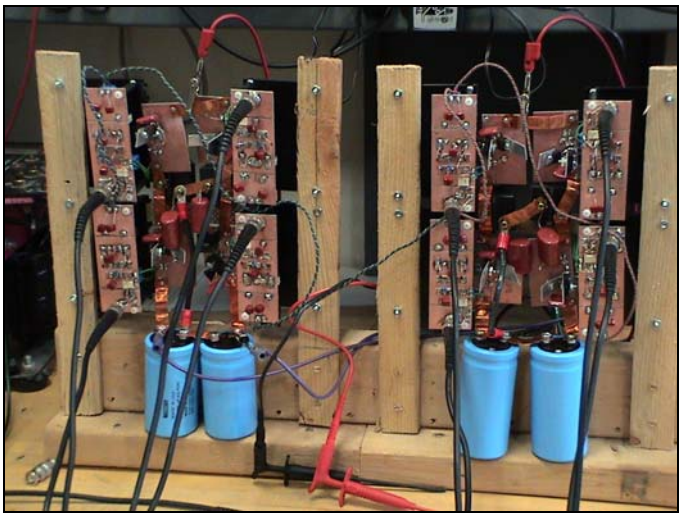


**Figure 4-18: One Phase of the CMLC**

## K. SUMMARY

This chapter documented the design and construction of the power supply operational amplifier, the power unit and its associated circuit cards and finally the cascaded multi-level converter. The next chapter contains a description of the design and construction of the digital logic section that controls the switching of the CMLC's transistors to create an ac sine-wave from a dc voltage source.

# V. DIGITAL LOGIC CONTROL OF CMLC

## A. PURPOSE

This chapter documents the design and formulation of the digital logic control circuit which executes the switching of the CMLC transistors. Some prominent alternative switching techniques are briefly discussed.

## B. DESCRIPTION/BACKGROUND OF CMLC SWITCHING TECHNIQUES

One technique that may be used to control the gating of a three-level converter is sine-triangle pulse-width-modulation (STPWM). The concept of STPWM involves the production of a sinusoidal output voltage waveform at a desired frequency by comparing a sinusoidal control signal, set at the desired frequency, with a triangular waveform. Figure 5-1 provides a graphical representation of this concept.

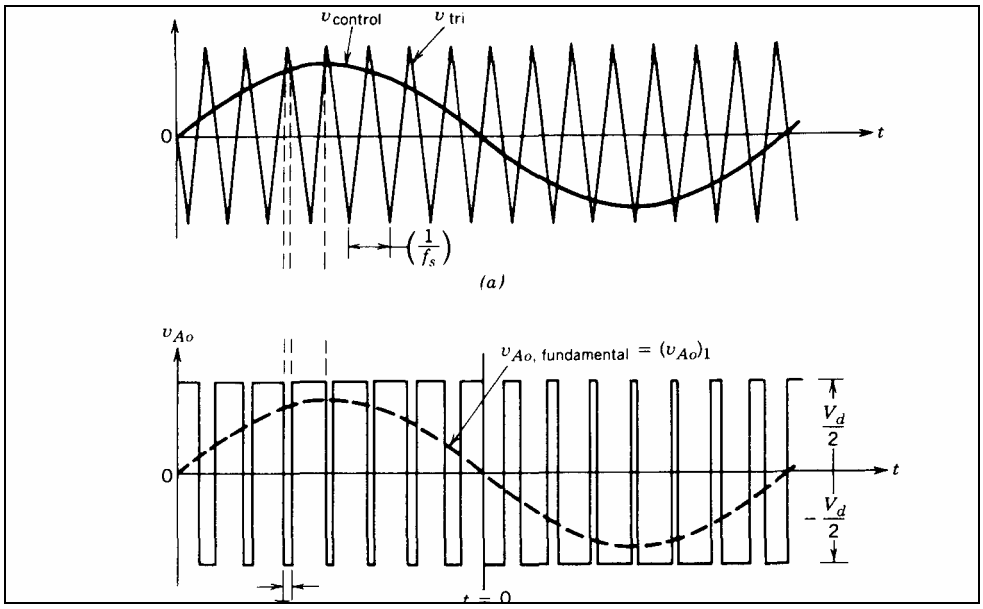



**Figure 5-1: Sine-Triangle Pulse Width Modulation [From Ref. 5.]**

In Figure 5-1 [5], the upper graph shows the sinusoidal control waveform ($v_{control}$) and the triangle waveform ($v_{tri}$) for one phase of a three-level converter. The important aspect of this technique is the intersection of the sinusoid and the triangle waveforms. During operation, when an intersection is detected, the corresponding converter transistors are

gated ‘on’ or ‘off’ depending on whether $v_{control}$ is greater than or less than $v_{tri}$. This ‘intersection detection’ gating is shown in the lower portion of Figure 5-1.

The major advantages of using STPWM are that the harmonics are significantly reduced and the fundamental frequency is controlled. When the carrier frequency ($v_{control}$) is much greater than the modulating frequency ($v_{tri}$), harmonics are generated along the high end of the frequency spectrum and thus away from the desired fundamental frequency (in most practical cases, 60 Hz). The major disadvantages of this method are that the modulating signals must be generated and the intersection of these signals monitored.

Another technique that may be used for transistor gating is the Space Vector Modulation (SVM) technique. The SVM method involves the transformation of each converter state (all three phases) into a single point on a q-d stationary frame. This transformation is executed by using the following equation (5-1).

$$\begin{bmatrix} V_{qs}^{s} \\ V_{ds}^{s} \end{bmatrix} = \begin{vmatrix} 1 & 0 & 0 \\ 0 & \frac{-\sqrt{3}}{3} & \frac{\sqrt{3}}{3} \end{vmatrix} \begin{bmatrix} V_{as} \\ V_{bs} \\ V_{cs} \end{bmatrix} \tag{5-1}$$

Figure 5-2 is a representation of a four-level converter q-d stationary frame and the possible converter states are represented as black dots.

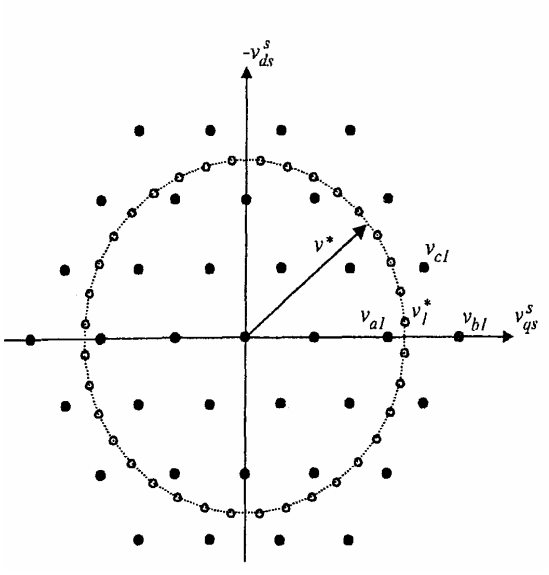



**Figure 5-2: Space Vector Modulation for the Four-Level Converter [From Ref. 4.]**

In Figure 5-2, the circular trace, with the equally spaced small black circles, represents a desired balanced set of output voltages and is called the reference trajectory; the number of black circles determines the switching frequency of the converter. Although the path could be arbitrary, a circular reference trajectory is chosen in the q-d plane since it results in balanced three-phase sinusoidal voltages in the time domain. The SVM technique attempts to synthesize the reference trajectory by averaging the amount of time spent at the three nearest states of each reference trajectory dot.

SVM allows for the utilization of more of the bus or dc-link voltage and it lowers commutation losses [3, 4, 8]. SVM is a method of choice to control modern power electronics circuits. This technique was considered for use in this thesis circuit; however, the time needed to build the controller due to its complex design forced an alternative method to be chosen.

The digital logic design method used for this project is a simple, straightforward method chosen to ensure that the converter was controlled with a hard-wired state sequencer that would minimize the testing of the controller itself and optimize the testing of the CMLC.

## C. FORMULATION OF DIGITAL LOGIC CONTROL ALGORITHM FOR CMLC

The CMLC designed in this project was configured to operate at nine different voltage levels from –4E volts to +4E volts (where E is the standard DC voltage increment of the CMLC). The first step in the design of the logic was the digitization of a sine-wave into nine different levels throughout an index integer range of 0 to 35.

For this process, an index range of 36 was selected in order to achieve a digital system requiring a clock that sequences through no more than a six-digit number system. Sub-dividing the sine-wave with a larger index range would definitely enhance the resolution of the wave pattern; however, a larger index range will require a more expensive and more complex digital circuit. A higher resolution sine-wave is desirable; however, the additional effort would bring this thesis work beyond the scope originally

specified. The introduction of a more complex converter controller is discussed later as potential follow-on work in this area.

The equation that was used to accomplish the digitization of the sine-wave is

$$\mathrm{INT}\left(4-(4)\sin\left(\mathrm{index}\left(\frac{\pi}{18}\right)\right)+0.5\right). \tag{5-2}$$

The equation was implemented in an EXCEL spreadsheet function where the INT command ensures that the results are integers and index = {0:35}. The results are presented in Table 5-1 and then graphically displayed in Figure 5-3.

| Index | Volt | Index | Volt | Index | Volt | Index | Volt | Index | Volt |
|---|---|---|---|---|---|---|---|---|---|
| 0 | 4 | 8 | 0 | 16 | 3 | 24 | 7 | 32 | 7 |
| 1 | 3 | 9 | 0 | 17 | 3 | 25 | 8 | 33 | 6 |
| 2 | 3 | 10 | 0 | 18 | 4 | 26 | 8 | 34 | 5 |
| 3 | 2 | 11 | 0 | 19 | 5 | 27 | 8 | 35 | 5 |
| 4 | 1 | 12 | 1 | 20 | 5 | 28 | 8 | | |
| 5 | 1 | 13 | 1 | 21 | 6 | 29 | 8 | | |
| 6 | 1 | 14 | 1 | 22 | 7 | 30 | 7 | | |
| 7 | 0 | 15 | 2 | 23 | 7 | 31 | 7 | | |

**Table 5-1: Digitized Sine-Wave Voltage Levels**

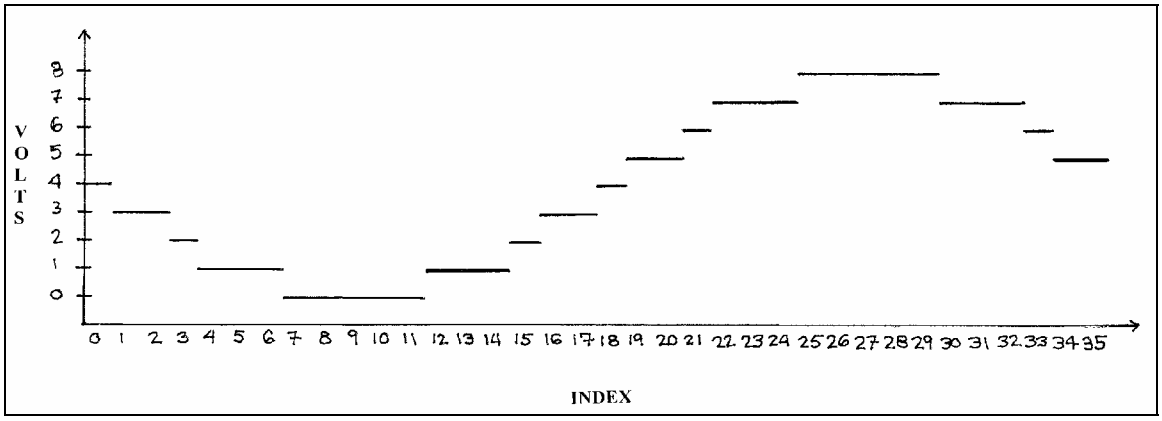



**Figure 5-3: Digitized Sinusoidal Waveform**

Once the sine-wave was digitized, a digital counter was designed. Using the same index range {0:35}, a six-digit counter was constructed. An important design parameter of the desired digital counter is the ability to avoid certain transistor sequences that would

put the converter in an unsafe condition (e.g., all phase A transistors fired at once causing a short). To ensure unsafe converter conditions were avoided, the use of two grey-scale counters was introduced into the design. A grey-scale counter simply counts through a pre-programmed sequence and it does so in such a manner that only one bit changes each time it sequences [9].

As mentioned above, the grey-scale counter sequence is purposely void of unsafe and unnecessary configurations. In this case, the two conditions are 000 and 111. The counter sequence of each counter was programmed as follows:

$$001 \rightarrow 011 \rightarrow 010 \rightarrow 110 \rightarrow 100 \rightarrow 101.$$

The combined grey-scale counters will then sequence from 001001 to 101101 and never exhibit an unsafe or unnecessary sequence. Table 5-2 displays the entire sequence and shows the configuration or voltage level of the transistor at each sequence index. As the digital counter counts through the sequence, displayed in Table 5-2, it signals the digital logic section which outputs the appropriate phase configuration based on the digital counter signal that is received. This phase configuration digital logic section is a four-digit output sent to the eight transistors that comprises each phase.

| Counter # | Phase A | Phase B | Phase C | Index |
|---|---|---|---|---|
| 001001 | 01100110 | 11000110 | 00110110 | 0 |
| 001011 | 01101100 | 11000011 | 00110110 | 1 |
| 001010 | 01101100 | 11000011 | 00110110 | 2 |
| 001110 | 00110011 | 11000011 | 00110011 | 3 |
| 001100 | 00110110 | 11000011 | 01101100 | 4 |
| 001101 | 00110110 | 11000011 | 01101100 | 5 |
| 011001 | 00110110 | 11000110 | 01100110 | 6 |
| 011011 | 00111100 | 11000110 | 01100011 | 7 |
| 011010 | 00111100 | 11000110 | 01100011 | 8 |
| 011110 | 00111100 | 11000011 | 11001100 | 9 |
| 011100 | 00111100 | 01100011 | 11000110 | 10 |
| 011101 | 00111100 | 01100011 | 11000110 | 11 |
| 010001 | 00110110 | 01100110 | 11000110 | 12 |
| 010011 | 00110110 | 01101100 | 11000011 | 13 |
| 010010 | 00110110 | 01101100 | 11000011 | 14 |
| 010110 | 00110011 | 00110011 | 11000011 | 15 |
| 010100 | 01101100 | 00110110 | 11000011 | 16 |
| 010101 | 01101100 | 00110110 | 11000011 | 17 |
| 110001 | 01100110 | 00110110 | 11000110 | 18 |
| 110011 | 01100011 | 00111100 | 11000110 | 19 |
| 110010 | 01100011 | 00111100 | 11000110 | 20 |
| 110110 | 11001100 | 00111100 | 11000011 | 21 |
| 110100 | 11000110 | 00111100 | 01100011 | 22 |
| 110101 | 11000110 | 00111100 | 01100011 | 23 |
| 100001 | 11000110 | 00110110 | 01100110 | 24 |
| 100011 | 11000011 | 00110110 | 01101100 | 25 |
| 100010 | 11000011 | 00110110 | 01101100 | 26 |
| 100110 | 11000011 | 00110011 | 00110011 | 27 |
| 100100 | 11000011 | 01101100 | 00110110 | 28 |
| 100101 | 11000011 | 01101100 | 00110110 | 29 |
| 101001 | 11000110 | 01100110 | 00110110 | 30 |
| 101011 | 11000110 | 01100011 | 00111100 | 31 |
| 101010 | 11000110 | 01100011 | 00111100 | 32 |
| 101110 | 11000011 | 11001100 | 00111100 | 33 |
| 101100 | 01100011 | 11000110 | 00111100 | 34 |
| 101101 | 01100011 | 11000110 | 00111100 | 35 |

**Table 5-2: Digital Logic Sequence for Three-Phase Converter**

It was conveniently discovered while researching the cascaded multi-level converter that, during operation, the transistors required a complementary logic sequence. Referring to Figure 5-4, the complementary transistor pairs are: $T_1$ and $T_3$, $T_2$ and $T_4$, $T_{1X}$ and $T_{3X}$, and $T_{2X}$ and $T_{4X}$. Therefore, one half of the phase transistors require direct input from this digital logic section, whereas the other half of the transistors requires the inverted version of the signal.

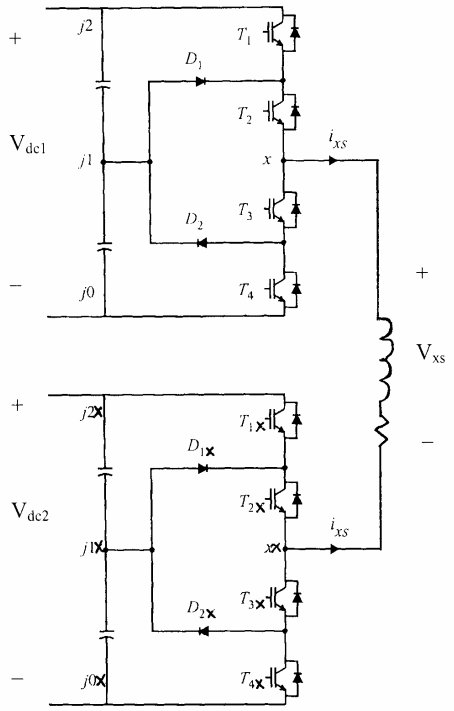



**Figure 5-4: One Phase of CMLC [From Ref. 3.]**

## D. PROGRAMMING OF PLD CHIPS

Advanced Boolean Expression Language (ABEL) software was used to program the counters and the converter configuration states. Appendices B-1, B-2, and B-3 contain the ABEL code for phases A, B and C of the CMLC. A default condition was included for each phase. Even though a safe-guard was added with the use of grey-scale counter, further precaution was taken by making all possible bad or unneeded CLMC

states (000 and 111) be assigned a default configuration of "0101" which automatically switches the circuit to the ground state.

Once the code was verified through the use of the ABEL test vector module, the software was loaded into the Progammable-Logic Device Progamming system. The PLD components used were the 20-pin, P18CV8 chips. One PLD was programmed as the digital counter and three PLDs were programmed as the Phase A, B and C chips containing the proper converter configuration information needed to produce the desired sine-wave for each phase.

## E. DESIGN AND BUILD OF THE DIGITAL LOGIC CIRCUIT

The digital-logic circuit was constructed on a PB-503 "proto-board" which provides TTL Signal Generator (clock), ground and 5 V signals needed to power each device. Figure 5-5 shows the circuit for one phase. The TTL Signal Generator (variable frequency) inputs into the six-digit digital counter (two grey-scale counters). The output from the counter feeds into the Phase PLD. The four-digit output of the Phase PLD is the signal that is sent to the input of each gate driver circuit card opto-coupler which in turn gates the accompanying IGBT. As discussed in sub-section C, four transistors receive the direct output (T1, T2, T1X, T2X) from the Phase PLD and the other four transistors receive an inverted version of the output ($\overline{T1}$, $\overline{T2}$, $\overline{T1X}$, $\overline{T2X}$) via an inverter chip.

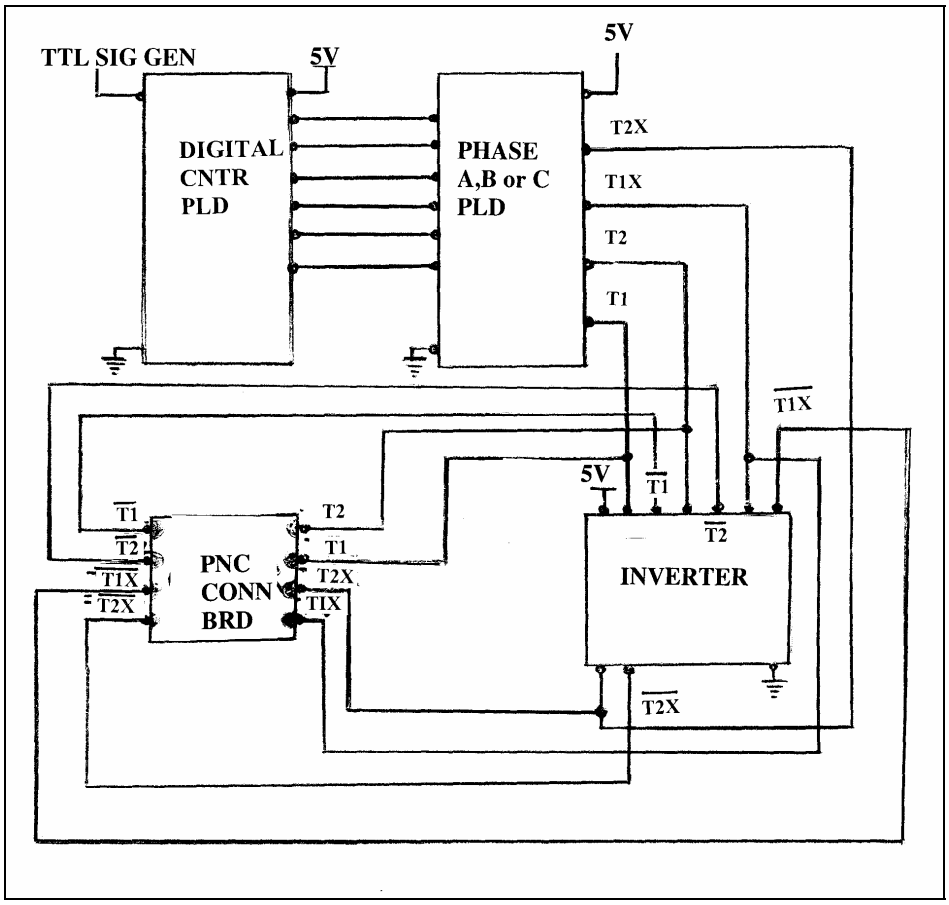



**Figure 5-5: Digital Logic Circuit for One Converter Phase**

## F. TESTING OF DIGITAL LOGIC CIRCUIT

The digital logic circuit, shown in Figure 5-5, was tested prior to its installment into the overall converter circuit. The frequency of the TTL Signal Generator was decreased to 1 Hz and with the output of the Phase PLD diverted to a bank of LEDs. Each converter configuration was verified as the circuit sequenced from indices 0 to 35. Each Phase PLD was tested and all sequences were verified as accurate.

## G. SUMMARY

This chapter presented a broad overview of the alternative techniques used to control modern power electronic circuits and then the design, implementation and testing of a digital logic controller was described. The next chapter, Chapter VI, documents the testing of the CMLC.

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# VI. TESTING OF CMLC

## A. PURPOSE

The purpose of this chapter is the documentation of all test results conducted on the Cascaded Multi-Level Converter (CMLC). All testing was accomplished at the NPS Power Laboratory with available lab equipment.

## B. BACKGROUND

Prior to the final assembly of the CMLC, each of the following circuits/modules were tested:

- Power Unit module,
- Operational Amplifier Power Supply, and
- Digital Logic Switching Circuit.

Each power unit module (discussed in Chapter IV) was given a post-construction test. The test circuit, shown in Figure 6-1, consisted of a resistor load placed in series with a 5-VDC voltage source, a function generator and a differential amplifier probe and oscilloscope measuring configuration. The IGBT of the power unit was placed in series with the resistor and dc voltage source, and a 10 kHz, 5-volt square-wave, provided by the function generator, was connected to the input of the opto-coupler device. The differential amplifier probes were place across the IGBT collector and emitter. The power unit module was deemed satisfactory when the IGBT generated a 10 kHz, 5-volt square-wave pattern.

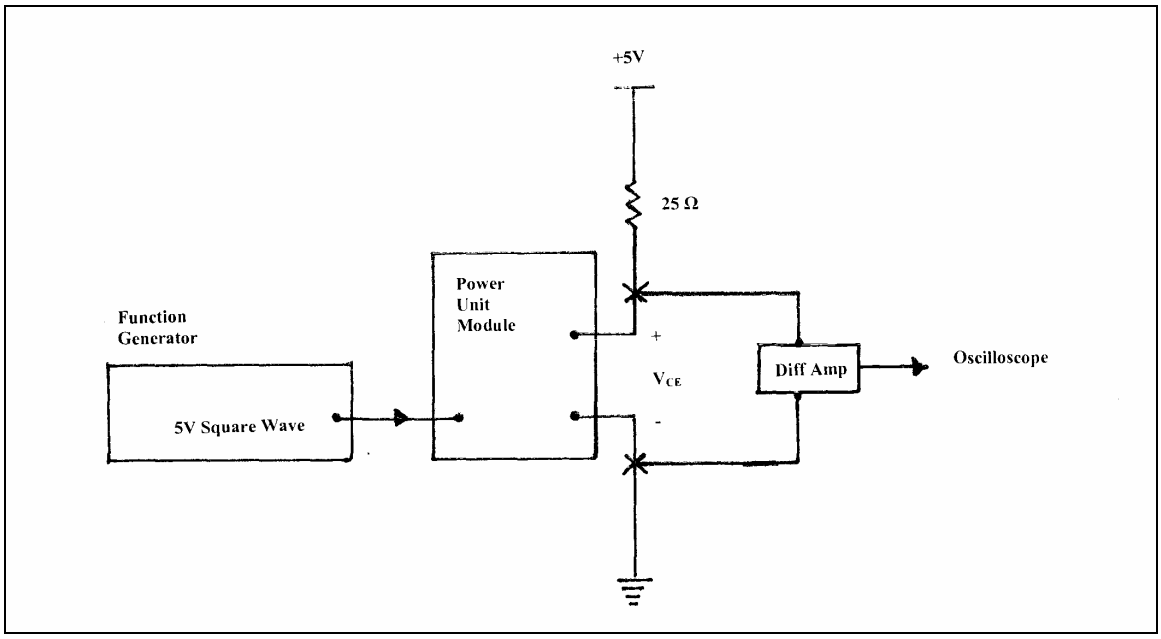


**Figure 6-1: Power Unit Module Test Circuit**

The operational amplifier power supply was first tested with one bank of eight interconnected power unit modules as the power supply load. The test was satisfactory. The 20 kHz, 30 VAC peak-to-peak voltage output from the power supply appeared across the input of each power unit module and there was no distortion detected. The final testing involved the operational amplifier connected to all of the 24 power unit modules that make up the three phases of the CMLC. In this configuration, the voltage output suffered a resonance effect causing the output magnitude to pulse between 30 VAC peak-to-peak and 0 volts. This problem was corrected by adjusting the function generator output waveform from 20 kHz to 40 kHz. At 40 kHz, the operational amplifier provided a steady 30 VAC peak-to-peak voltage output.

The digital logic switching circuit test was discussed in Chapter V. Additional testing involving this circuit was conducted to verify that all three phase programmable logic devices operated correctly.

## C. TESTING

The following tests were conducted on the CMLC:

- Single phase – low voltage/low current,
- Two phases – low voltage/low current, and
- Three phases – high voltage/high current.

The tests were conducted in order, as listed above, to ensure that each phase segment of the converter operated correctly and to ensure that all phase segments operated in the proper phase sequence in a low-voltage, low-current condition, prior to operating the entire converter in a three-phase, high-voltage, high-current condition. Table 6-1 lists the equipment used to conduct all testing events.

**Table 6.1: Test Equipment List**

| Equipment | Parameters | Manufacturer | Part or Model Number |
|---|---|---|---|
| Oscilloscope | 100 MHz | TEKTRONIX | TDS 3012B |
| Oscilloscope | 4 Channel | TEKTRONIX | TDS 540 |
| Variac | 0-280 V, 25 A, 12.1 kVA | STACO | 2510-3 |
| Power-stat | 0-280 V, 15 A | SUPERIOR | 1001 |
| DC Power Supply | 0-30 V, 2A | TEKTRONIX | PS 280 |
| Power Diode Rectifier | | INVERPOWER | P101 DM |
| Filter Capacitor | | INVERPOWER | P106 FC |
| Function Generator | 11 MHz, 10 V, 2A | TEKTRONIX | CFG280 |
| Current Probe | | TEKTRONIX | TM502A |
| Inductor | 42.5 mH, 10 A | INVERPOWER | |
| Resistor Module | 3 kW | INVERPOWER | P108 RL |
| High Voltage Differential Probe | 1300 V / 130 V | TEKTRONIX | P5200 |
| Multi-meter, Hand-held | | EXTECH | Multi-master 560 True RMS |

### 1. Low Voltage/Low Current Tests

The input voltage sources for the low voltage/low current tests consisted of two TEKTRONIX DC Power Supply units. Figure 6-2 shows the configuration of the power supply units and the CMLC. One power supply unit was configured to provide ± 30 VDC to the upper level of the CMLC and the second power supply unit was set-up to provide ± 10 VDC to the lower level of the CMLC.

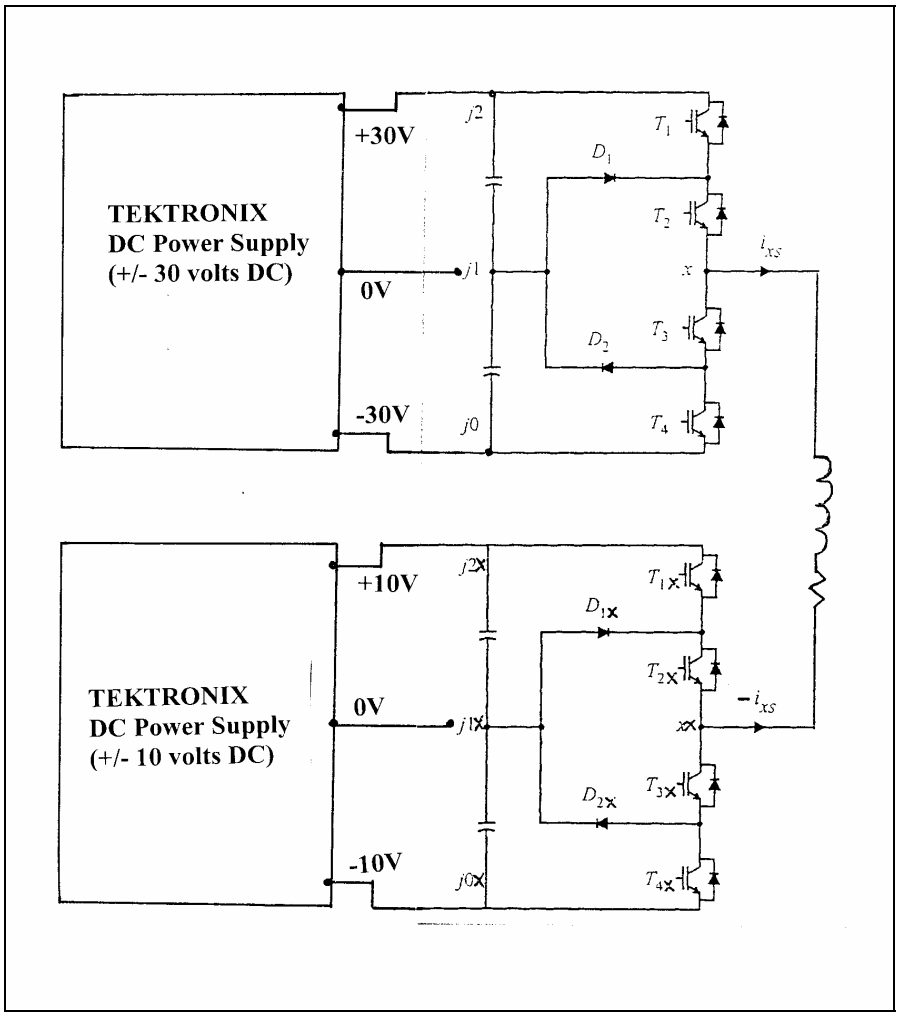


**Figure 6-2: Testing Configuration (Low Voltage/Low Current Condition)**

The load connected to the CMLC, during the low voltage/low current tests was a 42.5-mH inductor placed in series with a 60 Ω resistor bank on the resistor module. To match the impedance of the resistor and the inductor

$$f_{sw} = \frac{R_l}{2\pi L_l} = \frac{60\Omega}{2\pi(42.5\times10^{-3})} = 224.7 \text{ Hz}, \qquad (6.1)$$

was used to determine that the CMLC Digital Logic section must be operated at 224.7 Hz.

**a.** ***Single Phase – Low Voltage/Low Current Testing***

During the low voltage/low current test of CMLC's Phase 'A', 'B' and 'C', the current probe was adjusted to 0.5 A/Div and the high voltage differential probe was set at 1/500. Figure 6-3 is an oscilloscope digital image of CMLC Phase 'A' output voltage waveforms. One measurement was taken across the output terminals of the CMLC (chopped voltage waveform) and the second measurement was taken just across the load resistor (solid voltage waveform). The CMLC zero-to-peak voltage output waveform measured as follows:

-- 1.52 Divisions x 50.0 mV/Divisions = 75.0 mV (Actual oscilloscope output)

-- 76.0 mV x 500 = 38 V (Differential amplifier correction)

The 38 V output compares closely to the maximum voltage (expected) of 40 V as calculated in

$$\text{Maximum voltage (expected)} = 3\text{E} - (-1\text{E}) = \frac{4\text{E}}{2} = 40 \text{ volts}, \qquad (6\text{-}2)$$

where E = 20 V. The difference between expected and actual values is attributed to the rated total switching loss of each transistor in the circuit. This difference in values will be present throughout all testing phases. The expected voltage across the resistor was 28.3 V as calculated in

$$R_{load} = \sqrt{Z_L{}^2 + Z_R{}^2} = \sqrt{60.0^2 + 60.0^2} = 84.85\ \Omega, \qquad (6\text{-}3)$$

$$i_{as} = \frac{v_{as}}{R_{load}} = \frac{40}{84.85} = 0.471 \text{ mA}, \qquad (6\text{-}4)$$

and

$$V_R = R_{load} i_{as} = 60\left(0.471\times10^{-3}\right) = 28.28 \text{ V}. \qquad (6\text{-}5)$$

(Note: The values calculated in Equations (6-4) and (6-5) are r.m.s. magnitudes)
The zero-to-peak voltage across the resistor (solid voltage waveform) measured as follows:

-- 1.05 x 50 mV/Div = 52.5 mV (Actual oscilloscope output)

-- 52.5 mV x 500 = 26.25 V (Differential amplifier correction)

The 26.3 V output (actual) compares closely with the expected value of 28.3 V. Figure 6-4 is an oscilloscope image of the output current ($i_{as}$) superimposed against the CMLC Output Voltage waveform. The measured value of the zero-to-peak output current was as follows:

-- 0.95 Division x 0.5 A/Division = 0.475 mA

This value compares closely to the expected current output of 0.471 mA. Table 6-2 shows the actual and expected values of each voltage and current measurement in Figures 6-3 and 6-4.

**Table 6-1: Phase 'A' Voltage and Current Measurements**

| | **Expected** | **Actual** |
|---|---|---|
| $V_{CMLC\ Output}$ | 40 V | 38 V |
| $V_{Resistor}$ | 28.3 V | 26.3 V |
| $i_{as}$ | 0.471 mA | 0.475 mA |

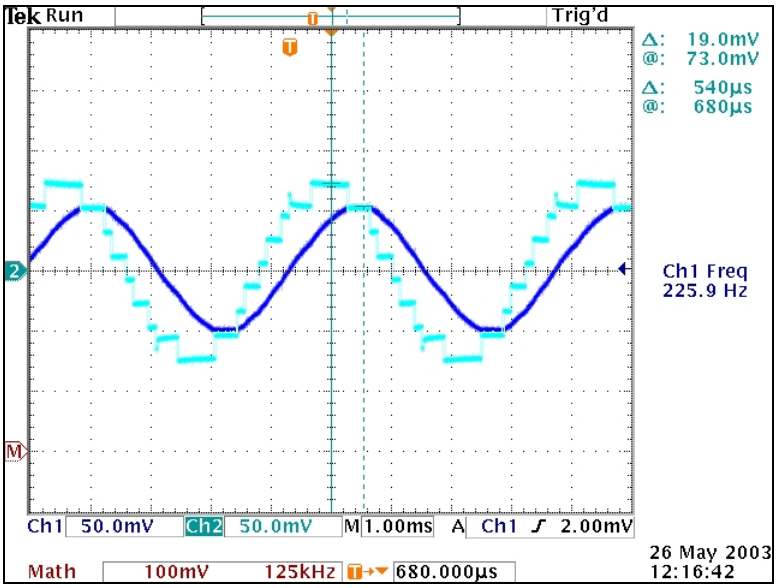


**Figure 6-3: Phase A Voltage Outputs (Chopped Waveform: Voltage Output of CMLC and Solid Waveform: Voltage Across Load Resistor)**

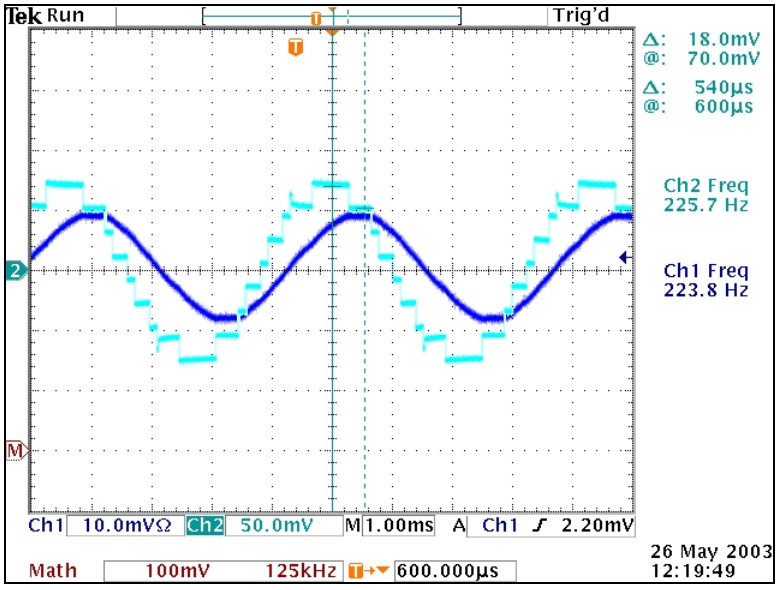


**Figure 6-4: Phase A Voltage and Current Output (Solid Waveform: Output Current and Chopped Waveform: Voltage Across CMLC Output)**

Figures 6-5 thru 6-8 are the oscilloscope images for phases B and C. Table 6-2 displays the results of these measurements.

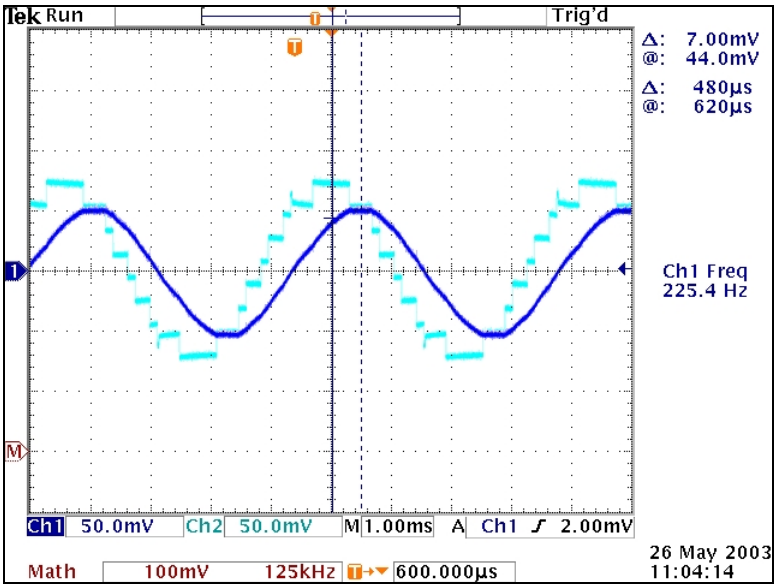


**Figure 6-5: Phase B Voltage Outputs (Chopped Waveform: CMLC Output Voltage and Solid Waveform: Voltage across Load Resistor)**

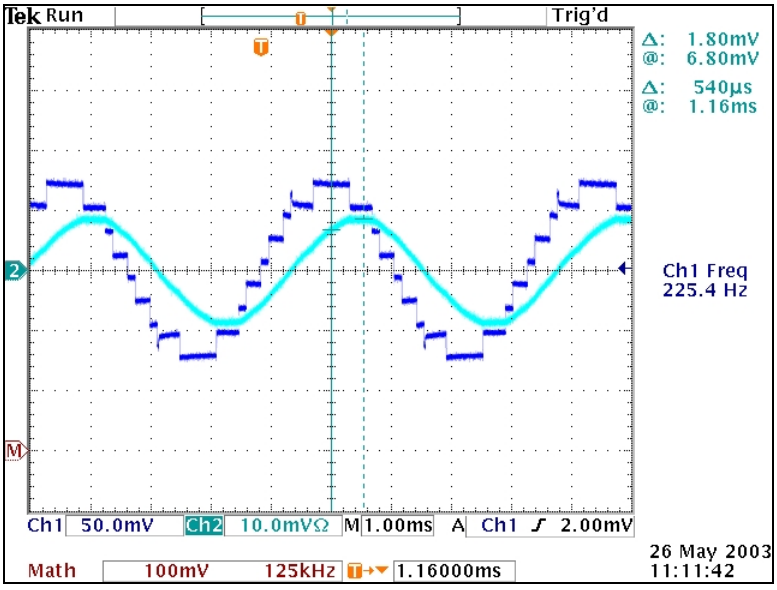


**Figure 6-6: Phase B Voltage and Current Output (Solid Waveform: Output Current and Chopped Waveform: CMLC Output Voltage)**

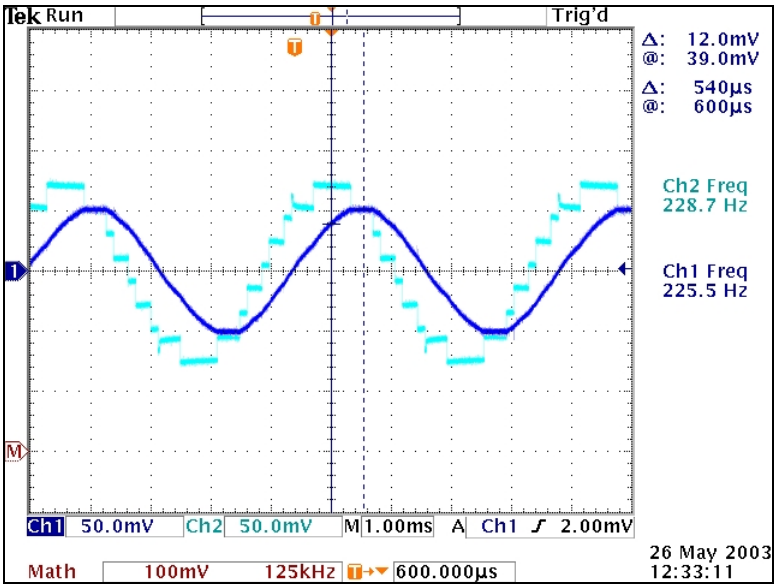


**Figure 6-7: Phase C Voltage Outputs (Chopped Waveform: CMLC Output Voltage and Solid Waveform: Voltage Across R)**

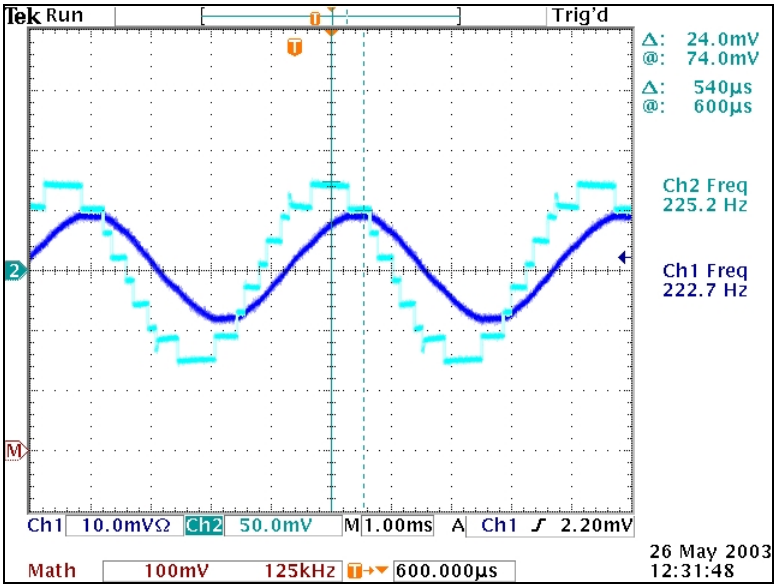


**Figure 6-8: Phase C Voltage and Current Output (Solid Waveform: Current and Chopped Waveform: CMLC Output Voltage)**

**Table 6-2: Voltage/Current Measurements for All Phases**

| | Expected | Measured |
|---|---|---|
| $V_{CMLC\ Output\ (PhA)}$ | 40 V | 38 V |
| $V_{Resistor\ (PhA)}$ | 28.3 V | 26.3 V |
| $i_{as}$ | 0.471 mA | 0.475 mA |
| $V_{CMLC\ Output(PhB)}$ | 40 V | 39 V |
| $V_{Resistor(PhB)}$ | 28.3 V | 27.5 V |
| $I_{bs}$ | 0.471 mA | 0.46 mA |
| $V_{CMLC\ Output(PhC)}$ | 40 V | 37.5 V |
| $V_{Resistor(PhC)}$ | 28.3 V | 27.5 V |
| $I_{cs}$ | 0.471 mA | 0.465 mA |

Transient waveforms were evident in the display of the CMLC output voltage for each phase. The transient 'overshoot' occurred on the voltage level just prior to the maximum and to the minimum voltage levels. This condition was considered a minor problem as it did not significantly disrupt the output current waveform. The cause of this transient effect seems to stem from the digital logic controller algorithm. This will be addressed in Chapter VII as a recommendation for future work on this circuit.

### b. *Two Phases – Low Voltage/Low Current Testing*

The testing of two phases simultaneously at low voltage and low current was conducted to ensure that the digital logic switching circuit was controlling the CMLC to produce three waveforms with 120º phase difference between them. The same testing equipment configuration used during single-phase testing was employed here. For purpose of clarification, the upper levels and lower levels of each CMLC phase are connected in parallel.

Figures 6-9 and 6-10 are oscilloscope images captured during this two-phase operation. Figure 6-9 is the voltage observed across the load resistors of phases 'A' and 'B.' To measure the phase difference between the two waveforms, a voltage peak from Phase A was centered on the y-axis and the oscilloscope's vertical cursor was placed at the Phase B voltage peak. The difference between the cursor and the y-axis measured 3.0 ms. The period of the two waveforms averaged at 225 Hz or 4.44 ms, and using

$$\angle\phi = \left(\frac{3.0}{4.44}\right) \times 360^{\circ} = 243^{\circ}, \qquad (6\text{-}6)$$

it was determined phases 'A' and 'B' were 243º out of phase. The same analysis was conducted on the phase 'A' and 'C' waveforms in Figure 6-10. It was determined that phase 'C' was 120.91º out of phase with phase 'A.'

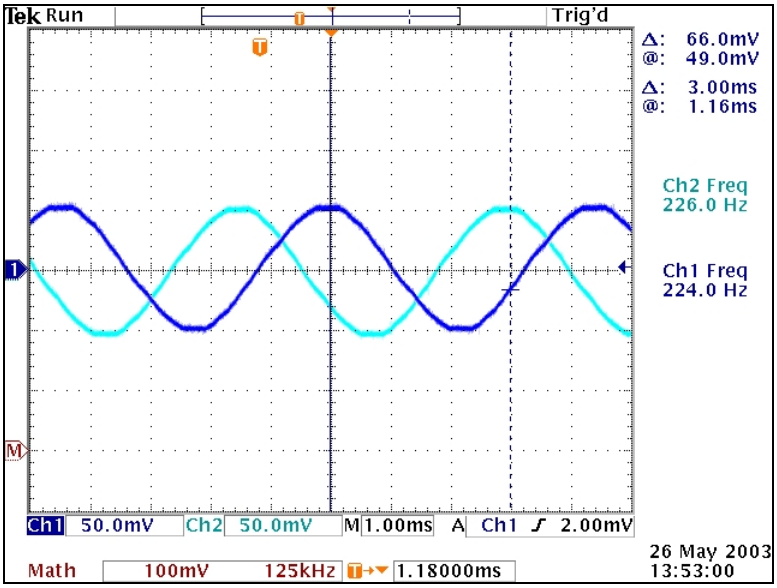


**Figure 6-9: Phases A & B: Output Voltage Across Resistor**

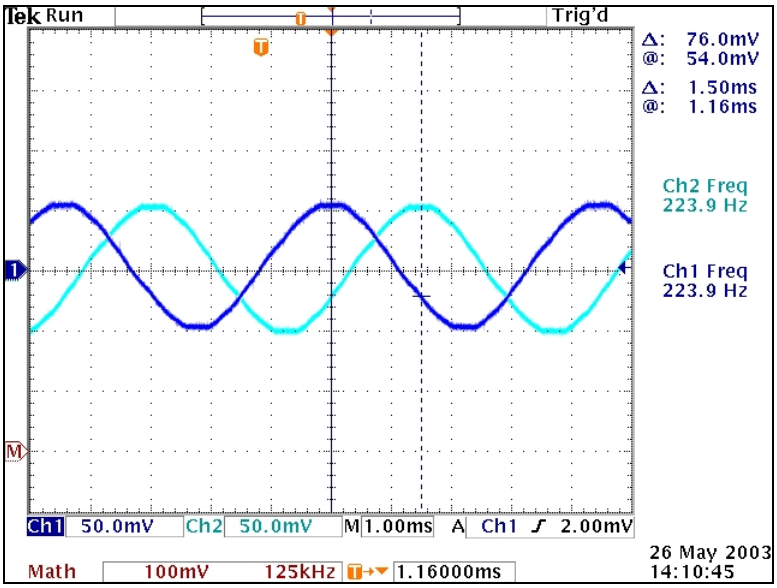


**Figure 6-10: Phases A & C Output Voltages (Across Resistor)**

### 2. High Voltage Test

The objective of the high voltage/ high current test was to operate the CMLC in three-phase configuration at a high voltage/high current condition and observe the resultant waveforms. The voltages applied across the upper and lower levels of the CMLC were set-up using the variac- and powerstat-voltage sources fed through the power rectifier and filter capacitor modules. The upper voltage was selected to be 270 V and the lower level voltage was established at 90 V (one-third the voltage of the upper level). To ensure the load resistor and inductor maintained matching impedance, the operating frequency was kept at 224.7 Hz. With these settings the expected voltage and current outputs (across the load resistor) were calculated at 180 V and 2.12 A using Equations (6-2) and (6-4) (where E = 90).

The TEKTRONIX Four Channel oscilloscope was used to capture the three-phase current outputs while in the high voltage/high current condition. The current probes connected to the oscilloscope were adjusted to 1.0 A/Division. Figure 6-11 represents a digital image of the oscilloscope current measurements. This zero-to-peak voltage was recorded at 178.5 V across the load resistor and the measured current was recorded at 2.1 A. Table 6-4 lists high voltage/high current condition results.

**Table 6-4: High Voltage/High Current Test Results**

| | **Expected** | **Measured** |
|---|---|---|
| $V_{CMLC}$ | 180 V | 178.5 V |
| Avg. Phase Current | 2.12 A | 2.10 A |

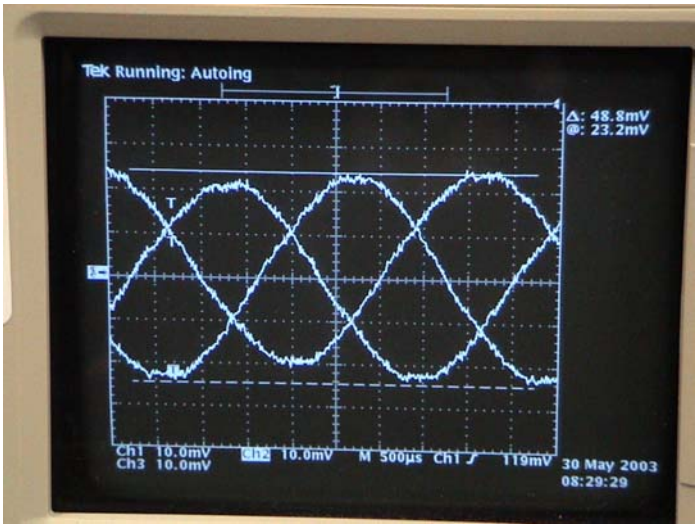


**Figure 6-11: Three Phase Current Output with Current Probe @ 1.0 A/DIV**

Following the prescribed testing plan, the input voltage levels were increased in 30 V and 10 V (upper and lower levels, respectively) increments to 360 V and 120 V (upper and lower levels, respectively). While the CMLC was in this configuration, an electric spark emanated from the upper level of the phase 'A' segment of the CMLC and the upper level voltage source circuit breaker opened. The CMLC was then disconnected to support troubleshooting in order to find out the cause of the casualty. The troubleshooting revealed a burned-out section on the snubber card of the "$T_1$" power unit module. Figure 6-12 is a digital image of the damaged card. It appeared that the damage was caused by the transistor collector-to-emitter current arcing over to the transistor gate path on the circuit card, creating a short and causing the power source circuit breaker to open. Further troubleshooting revealed no apparent damage to the circuit.

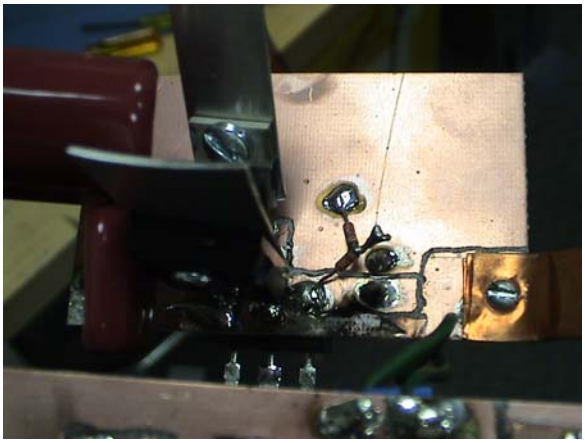

**Figure 6-12: Burned Out Section on $T_1$ Power Unit Snubber Card**

## D. SUMMARY

This chapter outlined the test results on the CMLC found in the laboratory. The following tests were conducted on the CMLC and CMLC components to verify proper operation:

- Power unit module test,
- Operational Amplifier Power Supply test,
- Digital Logic Switching Circuit test,
- CMLC single phase low voltage/low current test,
- CMLC two phases low voltage/low current test, and
- CMLC three phase high voltage/high current test.

In the final chapter, Chapter VII, project conclusions and accomplishments are addressed as well as possible follow-on opportunities.

# VII. CONCLUSIONS

## A. SUMMARY OF FINDINGS

This research documented the design and construction of a Cascaded Multi-Level Converter (CMLC). The key areas covered in the thesis are:

- Detailed schematics,
- Detailed component parts/manufacturer's lists,
- Documented component selection,
- Lab testing to validate design, and
- Converter layout.

The CMLC design process began with a component selection for the CMLC snubber circuit and gate driver circuit boards. Components were selected based on specifications provided by theoretical calculations and available components. Chapter III detailed the component selection process while Chapter IV documented the design of the CMLC Power Unit module components and the overall three phase CMLC circuit. Digital pictures were taken of each component built for the CMLC. Chapter V documented the design and testing of the Digital Logic Switching Circuit. Once construction was completed, the CMLC was tested in the power laboratory to ensure all components worked in low-voltage and high-voltage conditions.

## B. OBSERVATIONS

This thesis project was a labor- and time-intensive effort due to the amount of construction that was necessary. The building of the components and the overall circuit represented approximately 70% of the entire thesis effort. Table 7-1 shows the approximate amount of time spent for the construction portion of the project.

| TASK | TIME |
|---|---|
| -- Build Snubber Circuit Card. | 3.0 Hrs |
| -- Build Gate Driver Circuit Card | 5.0 Hrs |
| -- Assemble Power Unit Module | 1.0 Hrs |
| **Assemble 24 Power Unit Modules** | **216.0 Hrs** |
| | |
| -- Assemble CMLC Phase (8 Power Unit Modules/Phase) | 8.0 Hrs |
| **Assemble 3 CMLC Phases** | **24.0 Hrs** |
| | |
| -- Build Operational Amplifier Power Supply | 8.0 Hrs |

A considerable amount of time would have been saved by having a CAD-CAM system, capable of preparing circuit boards for population, available at NPS.

The CMLC hardware proved to be robust and durable. In order to tap the potential effectiveness of this converter topology, the digital logic controlling algorithm requires further research and refinement. This improvement should eliminate the present transient 'glitches' present in the current operation of the converter.

Further investigation into the casualty incurred during the post-testing high voltage operation revealed a design improvement that is needed to ensure reliable operation in future CMLC testing. The snubber circuit card layout needs to be redesigned in such a manner to ensure that the transistor gate region is moved further away from the transistor collector-to-emitter current region.

## C. FUTURE WORK

With CMLC technology offering high power conversion with reduced current waveform harmonics, continued research in dc-ac converters is vital for the future of naval ship electrical systems. Many issues still must be addressed in this design area. Possible areas for future research include:

- Development of Space Vector Modulation Switching Circuit,
- Development of Sine-Triangle Pulse Width Modulation Switching Circuit,
- Comparison of switching techniques,
- Use of CMLC in analysis of propulsion shaft transient noise, and
- The construction of a reduced-scale IPS at NPS to facilitate additional student thesis projects.

With IPS selected for DD(X), it is critical for research to continue in this area. DC-AC converters are an integral part of any electrical distribution system and the Navy must continue with research in this area to ensure successful and reliable systems are delivered to the fleet.

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## APENDIX A. DATA SHEETS

Appendix A contains data sheets for all the major components used to construct the operational amplifier power supply and the Cascaded Multi-Level Converter.

### A. NATIONAL SEMICONDUCTOR LM12CL 80W OP-AMP [From Ref. 12.]



National Semiconductor

May 1999

# LM12CL
# 80W Operational Amplifier

## General Description

The LM12 is a power op amp capable of driving ±25V at ±10A while operating from ±30V supplies. The monolithic IC can deliver 80W of sine wave power into a 4Ω load with 0.01% distortion. Power bandwidth is 60 kHz. Further, a peak dissipation capability of 800W allows it to handle reactive loads such as transducers, actuators or small motors without derating. Important features include:

- input protection
- controlled turn on
- thermal limiting
- overvoltage shutdown
- output-current limiting
- dynamic safe-area protection

The IC delivers ±10A output current at any output voltage yet is completely protected against overloads, including shorts to the supplies. The dynamic safe-area protection is provided by instantaneous peak-temperature limiting within the power transistor array.

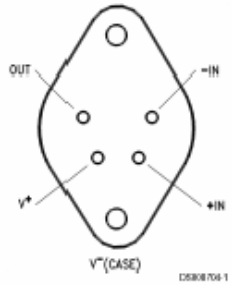
The turn-on characteristics are controlled by keeping the output open-circuited until the total supply voltage reaches 14V. The output is also opened as the case temperature exceeds 150˚C or as the supply voltage approaches the $BV_{CEO}$ of the output transistors. The IC withstands overvoltages to 80V.

This monolithic op amp is compensated for unity-gain feedback, with a small-signal bandwidth of 700 kHz. Slew rate is 9V/µs, even as a follower. Distortion and capacitive-load stability rival that of the best designs using complementary output transistors. Further, the IC withstands large differential input voltages and is well behaved should the common-mode range be exceeded.

The LM12 establishes that monolithic ICs can deliver considerable output power without resorting to complex switching schemes. Devices can be paralleled or bridged for even greater output capability. Applications include operational power supplies, high-voltage regulators, high-quality audio amplifiers, tape-head positioners, x-y plotters or other servo-control systems.

The LM12 is supplied in a four-lead, TO-3 package with V− on the case. A gold-eutectic die-attach to a molybdenum interface is used to avoid thermal fatigue problems. The LM12 is specified for either military or commercial temperature range.

## Connection Diagram

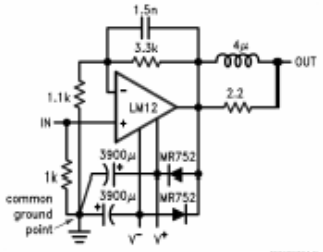



DS008704-1

4-pin glass epoxy TO-3 socket is available from AUGAT INC. Part number 8112-AG7

Bottom View
Order Number LM12CLK
See NS Package Number K04A

## Typical Application*




DS008704-2

*Low distortion (0.01%) audio amplifier

## Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

| | |
|---|---|
| Total Supply Voltage (Note 1) | 80V |
| Input Voltage | (Note 2) |
| Output Current | Internally Limited |
| Junction Temperature | (Note 3) |
| Storage Temperature Range | −65°C to 150°C |
| Lead Temperature (Soldering, 10 seconds) | 300°C |

## Operating Ratings

| | |
|---|---|
| Total Supply Voltage | 15V to 60V |
| Case Temperature (Note 4) | 0°C to 70°C |

## Electrical Characteristics (Note 4)

| Parameter | Conditions | Typ 25°C | LM12CL Limits | Units |
|---|---|---|---|---|
| Input Offset Voltage | $\pm 10V \le V_S \le \pm 0.5\ V_{MAX}$, $V_{CM} = 0$ | 2 | 15/20 | mV (max) |
| Input Bias Current | $V- + 4V \le V_{CM} \le V+ -2V$ | 0.15 | 0.7/1.0 | µA (max) |
| Input Offset Current | $V- +4V \le V_{CM} \le V+ -2V$ | 0.03 | 0.2/0.3 | µA (max) |
| Common Mode Rejection | $V- +4V \le V_{CM} \le V+ -2V$ | 86 | 70/65 | dB (min) |
| Power Supply Rejection | $V+ = 0.5\ V_{MAX}$, $-6V \ge V- \ge -0.5\ V_{MAX}$ | 90 | 70/65 | dB (min) |
| | $V- = -0.5\ V_{MAX}$, $6V \le V+ \le 0.5\ V_{MAX}$ | 110 | 75/70 | dB (min) |
| Output Saturation Threshold | $t_{ON} = 1$ ms, $\Delta V_{IN} = 5\ (10)$ mV, $I_{OUT} = 1A$ | 1.8 | 2.2/2.5 | V (max) |
| | 8A | 4 | 5/7 | V (max) |
| | 10A | 5 | | V (max) |
| Large Signal Voltage Gain | $t_{ON} = 2$ ms, $V_{SAT} = 2V$, $I_{OUT} = 0$ | 100 | 30/20 | V/mV (min) |
| | $V_{SAT} = 8V$, $R_L = 4\Omega$ | 50 | 15/10 | V/mV (min) |
| Thermal Gradient Feedback | $P_{DISS} = 50W$, $t_{ON} = 65$ ms | 30 | 100 | µV/W (max) |
| Output-Current Limit | $t_{ON} = 10$ ms, $V_{DISS} = 10V$ | 13 | 16 | A (max) |
| | $t_{ON} = 100$ ms, $V_{DISS} = 58V$ | 1.5 | 0.9/0.6 | A (min) |
| | | 1.5 | 1.7 | A (max) |
| Power Dissipation Rating | $t_{ON} = 100$ ms, $V_{DISS} = 20V$ | 100 | 80/55 | W (min) |
| | $V_{DISS} = 58V$ | 80 | 52/35 | W (min) |
| DC Thermal Resistance | (Note 5) $V_{DISS} = 20V$ | 2.3 | 2.9 | °C/W (max) |
| | $V_{DISS} = 58V$ | 2.7 | 4.5 | °C/W (max) |
| AC Thermal Resistance | (Note 5) | 1.6 | 2.1 | °C/W (max) |
| Supply Current | $V_{OUT} = 0$, $I_{OUT} = 0$ | 60 | 120/140 | mA (max) |

**Note 1:** Absolute maximum ratings indicate limits beyond which damage to the device may occur. The maximum voltage for which the LM12 is guaranteed to operate is given in the operating ratings and in Note 4. With inductive loads or output shorts, other restrictions described in applications section apply.

**Note 2:** Neither input should exceed the supply voltage by more than 50 volts nor should the voltage between one input and any other terminal exceed 60 volts.

**Note 3:** Operating junction temperature is internally limited near 225°C within the power transistor and 160°C for the control circuitry.

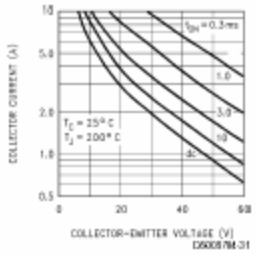
**Note 4:** The supply voltage is ±30V ($V_{MAX}$ = 60V), unless otherwise specified. The voltage across the conducting output transistor (supply to output) is $V_{DISS}$ and internal power dissipation is $P_{DISS}$. Temperature range is $0°C \le T_C \le 70°C$ where $T_C$ is the case temperature. Standard typeface indicates limits at 25°C **while boldface type refers to limits or special conditions over full temperature range.** With no heat sink, the package will heat at a rate of 35°C/sec per 100W of internal dissipation.

**Note 5:** This thermal resistance is based upon a peak temperature of 200°C in the center of the power transistor and a case temperature of 25°C measured at the center of the package bottom. The maximum junction temperature of the control circuitry can be estimated based upon a dc thermal resistance of 0.9°C/W or an ac thermal resistance of 0.6°C/W for any operating voltage.

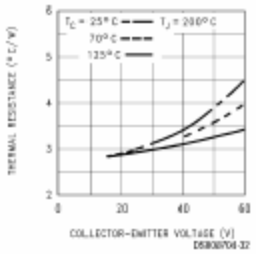
Although the output and supply leads are resistant to electrostatic discharges from handling, the input leads are not. The part should be treated accordingly.

## Output-Transistor Ratings (guaranteed)

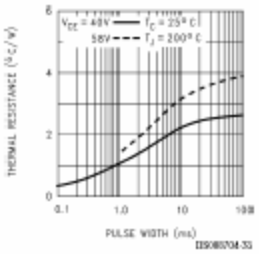
Safe Area




DC Thermal Resistance

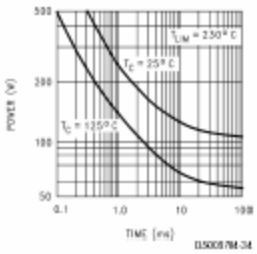



Pulse Thermal Resistance

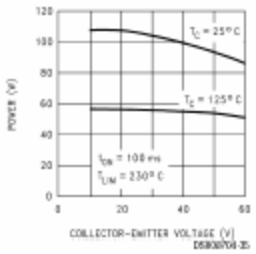



## Typical Performance Characteristics

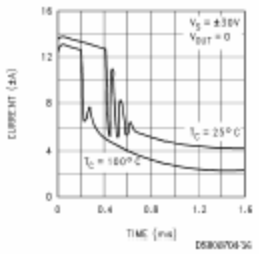
Pulse Power Limit



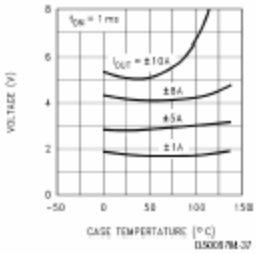

Pulse Power Limit



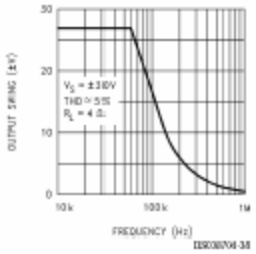

Peak Output Current



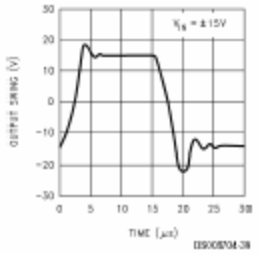

Output Saturation Voltage



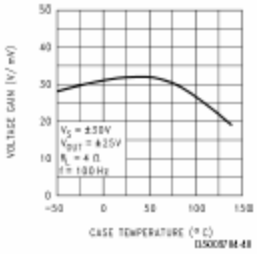

Large Signal Response



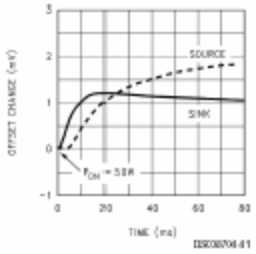

Follower Pulse Response



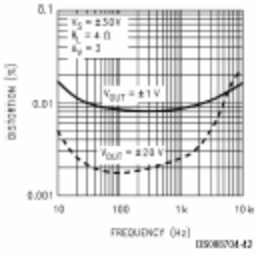

Large Signal Gain




Thermal Response

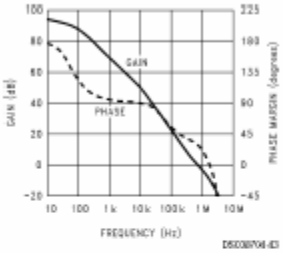



Total Harmonic Distortion

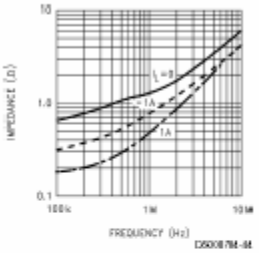


## Typical Performance Characteristics (Continued)

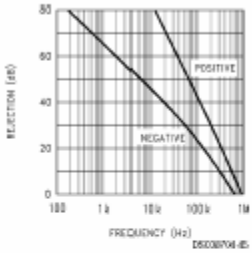
Frequency Response



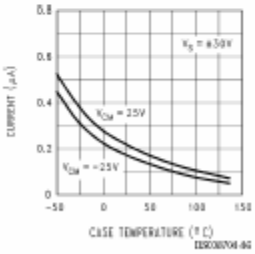

Output Impedance



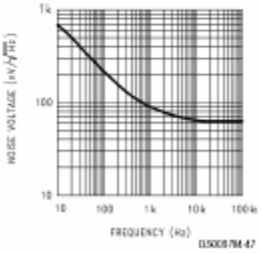

Power Supply Rejection



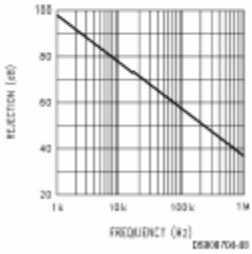

Input Bias Current



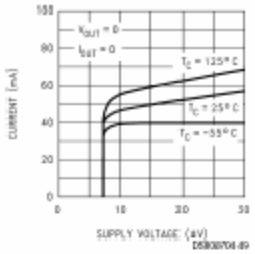

Input Noise Voltage



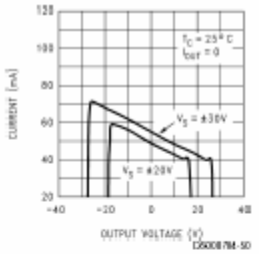

Common Mode Rejection



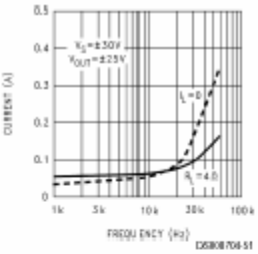

Supply Current




Supply Current




Cross-Supply Current




## Application Information

### GENERAL

Twenty five years ago the operational amplifier was a specialized design tool used primarily for analog computation. However, the availability of low cost IC op amps in the late 1960's prompted their use in rather mundane applications, replacing a few discrete components. Once a few basic principles are mastered, op amps can be used to give exceptionally good results in a wide range of applications while minimizing both cost and design effort.

The availability of a monolithic power op amp now promises to extend these advantages to high-power designs. Some conventional applications are given here to illustrate op amp design principles as they relate to power circuitry. The inevitable fall in prices, as the economies of volume production are realized, will prompt their use in applications that might now seem trivial. Replacing single power transistors with an op amp will become economical because of improved performance, simplification of attendant circuitry, vastly improved fault protection, greater reliability and the reduction of design time.

Power op amps introduce new factors into the design equation. With current transients above 10A, both the inductance and resistance of wire interconnects become important in a number of ways. Further, power ratings are a crucial factor in determining performance. But the power capability of the IC cannot be realized unless it is properly mounted to an adequate heat sink. Thus, thermal design is of major importance with power op amps.

This application summary starts off by identifying the origin of strange problems observed while using the LM12 in a

## Application Information (Continued)

wide variety of designs with all sorts of fault conditions. A few simple precautions will eliminate these problems. One would do well to read the section on supply bypassing, lead inductance, output clamp diodes, ground loops and reactive loading before doing any experimentation. Should there be problems with erratic operation, blow-outs, excessive distortion or oscillation, another look at these sections is in order.

The management and protection circuitry can also affect operation. Should the total supply voltage exceed ratings or drop below 15–20V, the op amp shuts off completely. Case temperatures above 150˚C also cause shut down until the temperature drops to 145˚C. This may take several seconds, depending on the thermal system. Activation of the dynamic safe-area protection causes both the main feedback loop to lose control and a reduction in output power, with possible oscillations. In ac applications, the dynamic protection will cause waveform distortion. Since the LM12 is well protected against thermal overloads, the suggestions for determining power dissipation and heat sink requirements are presented last.

### SUPPLY BYPASSING

All op amps should have their supply leads bypassed with low-inductance capacitors having short leads and located close to the package terminals to avoid spurious oscillation problems. Power op amps require larger bypass capacitors. The LM12 is stable with good-quality electrolytic bypass capacitors greater than 20 µF. Other considerations may require larger capacitors.

The current in the supply leads is a rectified component of the load current. If adequate bypassing is not provided, this distorted signal can be fed back into internal circuitry. Low distortion at high frequencies requires that the supplies be bypassed with 470 µF or more, at the package terminals.

### LEAD INDUCTANCE

With ordinary op amps, lead-inductance problems are usually restricted to supply bypassing. Power op amps are also sensitive to inductance in the output lead, particularly with heavy capacitive loading. Feedback to the input should be taken directly from the output terminal, minimizing common inductance with the load. Sensing to a remote load must be accompanied by a high-frequency feedback path directly from the output terminal. Lead inductance can also cause voltage surges on the supplies. With long leads to the power source, energy stored in the lead inductance when the output is shorted can be dumped back into the supply bypass capacitors when the short is removed. The magnitude of this transient is reduced by increasing the size of the bypass capacitor near the IC. With 20 µF local bypass, these voltage surges are important only if the lead length exceeds a couple feet (> 1 µH lead inductance). Twisting together the supply and ground leads minimizes the effect.

### GROUND LOOPS

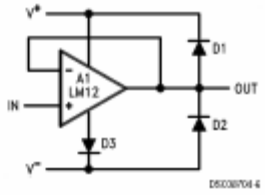
With fast, high-current circuitry, all sorts of problems can arise from improper grounding. In general, difficulties can be avoided by returning all grounds separately to a common point. Sometimes this is impractical. When compromising, special attention should be paid to the ground returns for the supply bypasses, load and input signal. Ground planes also help to provide proper grounding.

Many problems unrelated to system performance can be traced to the grounding of line-operated test equipment used for system checkout. Hidden paths are particularly difficult to sort out when several pieces of test equipment are used but can be minimized by using current probes or the new isolated oscilloscope pre-amplifiers. Eliminating any direct ground connection between the signal generator and the oscilloscope synchronization input solves one common problem.

### OUTPUT CLAMP DIODES

When a push-pull amplifier goes into power limit while driving an inductive load, the stored energy in the load inductance can drive the output outside the supplies. Although the LM12 has internal clamp diodes that can handle several amperes for a few milliseconds, extreme conditions can cause destruction of the IC. The internal clamp diodes are imperfect in that about half the clamp current flows into the supply to which the output is clamped while the other half flows across the supplies. Therefore, the use of external diodes to clamp the output to the power supplies is strongly recommended. This is particularly important with higher supply voltages.

Experience has demonstrated that hard-wire shorting the output to the supplies can induce random failures if these external clamp diodes are not used and the supply voltages are above ±20V. Therefore it is prudent to use output clamp diodes even when the load is not particularly inductive. This also applies to experimental setups in that blowouts have been observed when diodes were not used. In packaged equipment, it may be possible to eliminate these diodes, providing that fault conditions can be controlled.




Heat sinking of the clamp diodes is usually unimportant in that they only clamp current transients. Forward drop with 15A fault transients is of greater concern. Usually, these transients die out rapidly. The clamp to the negative supply can have somewhat reduced effectiveness under worst case conditions should the forward drop exceed 1.0V. Mounting this diode to the power op amp heat sink improves the situation. Although the need has only been demonstrated with some motor loads, including a third diode (D3 above) will eliminate any concern about the clamp diodes. This diode, however, must be capable of dissipating continuous power as determined by the negative supply current of the op amp.

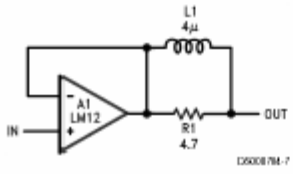
### REACTIVE LOADING

The LM12 is normally stable with resistive, inductive or smaller capacitive loads. Larger capacitive loads interact with the open-loop output resistance (about 1Ω) to reduce the phase margin of the feedback loop, ultimately causing oscillation. The critical capacitance depends upon the feedback applied around the amplifier; a unity-gain follower can handle about 0.01 µF, while more than 1 µF does not cause problems if the loop gain is ten. With loop gains greater than unity, a speedup capacitor across the feedback resistor will

## Application Information (Continued)

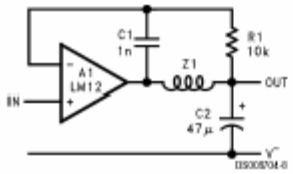
aid stability. In all cases, the op amp will behave predictably only if the supplies are properly bypassed, ground loops are controlled and high-frequency feedback is derived directly from the output terminal, as recommended earlier.

So-called capacitive loads are not always capacitive. A high-Q capacitor in combination with long leads can present a series-resonant load to the op amp. In practice, this is not usually a problem; but the situation should be kept in mind.




D5008784-7

Large capacitive loads (including series-resonant) can be accommodated by isolating the feedback amplifier from the load as shown above. The inductor gives low output impedance at lower frequencies while providing an isolating impedance at high frequencies. The resistor kills the Q of series resonant circuits formed by capacitive loads. A low inductance, carbon-composition resistor is recommended. Optimum values of L and R depend upon the feedback gain and expected nature of the load, but are not critical. A 4 µH inductor is obtained with 14 turns of number 18 wire, close spaced, around a one-inch-diameter form.




D5008784-8

The LM12 can be made stable for all loads with a large capacitor on the output, as shown above. This compensation gives the lowest possible closed-loop output impedance at high frequencies and the best load-transient response. It is appropriate for such applications as voltage regulators.

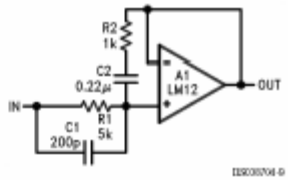
A feedback capacitor, $C_1$, is connected directly to the output pin of the IC. The output capacitor, $C_2$, is connected at the output terminal with short leads. Single-point grounding to avoid dc and ac ground loops is advised.

The impedance, $Z_1$, is the wire connecting the op amp output to the load capacitor. About 3-inches of number-18 wire (70 nH) gives good stability and 18-inches (400 nH) begins to degrade load-transient response. The minimum load capacitance is 47 µF, if a solid-tantalum capacitor with an equivalent series resistance (ESR) of 0.1Ω is used. Electrolytic capacitors work as well, although capacitance may have to be increased to 200 µF to bring ESR below 0.1Ω.

Loop stability is not the only concern when op amps are operated with reactive loads. With time-varying signals, power dissipation can also increase markedly. This is particularly true with the combination of capacitive loads and high-frequency excitation.

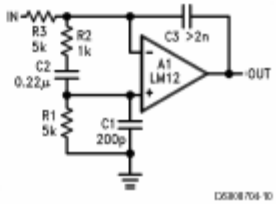
### INPUT COMPENSATION

The LM12 is prone to low-amplitude oscillation bursts coming out of saturation if the high-frequency loop gain is near unity. The voltage follower connection is most susceptible. This glitching can be eliminated at the expense of small-signal bandwidth using input compensation. Input compensation can also be used in combination with LR load isolation to improve capacitive load stability.




D5008784-9

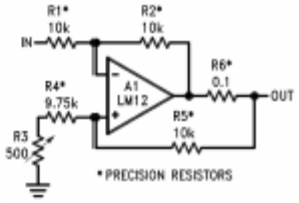
An example of a voltage follower with input compensation is shown here. The $R_2C_2$ combination across the input works with $R_1$ to reduce feedback at high frequencies without greatly affecting response below 100 kHz. A lead capacitor, $C_1$, improves phase margin at the unity-gain crossover frequency. Proper operation requires that the output impedance of the circuitry driving the follower be well under 1 kΩ at frequencies up to a few hundred kilohertz.




D5008784-10

Extending input compensation to the integrator connection is shown here. Both the follower and this integrator will handle 1 µF capacitive loading without LR output isolation.

### CURRENT DRIVE

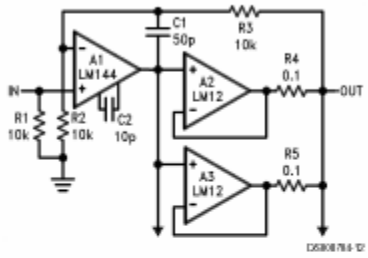



D5008784-11

This circuit provides an output current proportional to the input voltage. Current drive is sometimes preferred for servo motors because it aids in stabilizing the servo loop by reducing phase lag caused by motor inductance. In applications requiring high output resistance, such as operational power supplies running in the current mode, matching of the feedback resistors to 0.01% is required. Alternately, an adjustable resistor can be used for trimming.

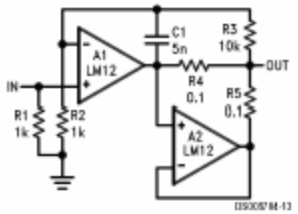
## Application Information (Continued)

PARALLEL OPERATION




Output drive beyond the capability of one power amplifier can be provided as shown here. The power op amps are wired as followers and connected in parallel with the outputs coupled through equalization resistors. A standard, high-voltage op amp is used to provide voltage gain. Overall feedback compensates for the voltage dropped across the equalization resistors.

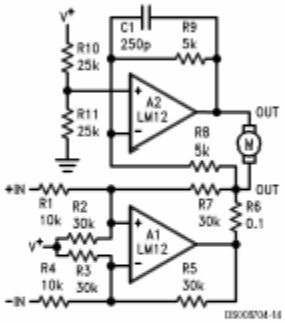
With parallel operation, there may be an increase in unloaded supply current related to the offset voltage across the equalization resistors. More output buffers, with individual equalization resistors, may be added to meet even higher drive requirements.




This connection allows increased output capability without requiring a separate control amplifier. The output buffer, $A_2$, provides load current through $R_5$ equal to that supplied by the main amplifier, $A_1$, through $R_4$. Again, more output buffers can be added.

Current sharing among paralleled amplifiers can be affected by gain error as the power-bandwidth limit is approached. In the first circuit, the operating current increase will depend upon the matching of high-frequency characteristics. In the second circuit, however, the entire input error of $A_2$ appears across $R_4$ and $R_5$. The supply current increase can cause power limiting to be activated as the slew limit is approached. This will not damage the LM12. It can be avoided in both cases by connecting $A_1$ as an inverting amplifier and restricting bandwidth with $C_1$.

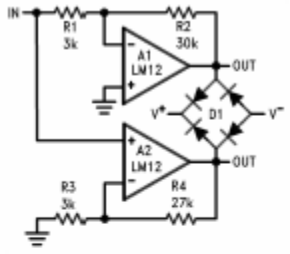
SINGLE-SUPPLY OPERATION




Although op amps are usually operated from dual supplies, single-supply operation is practical. This bridge amplifier supplies bi-directional current drive to a servo motor while operating from a single positive supply. The output is easily converted to voltage drive by shorting $R_6$ and connecting $R_7$ to the output of $A_2$, rather than $A_1$.

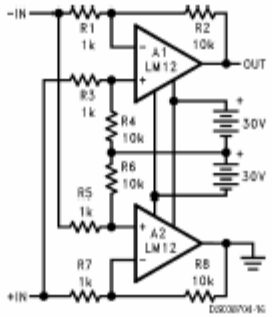
Either input may be grounded, with bi-directional drive provided to the other. It is also possible to connect one input to a positive reference, with the input signal varying about this voltage. If the reference voltage is above 5V, $R_2$ and $R_3$ are not required.

HIGH VOLTAGE AMPLIFIERS

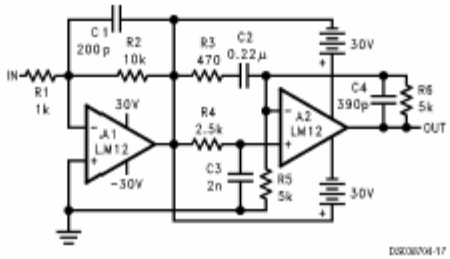



The voltage swing delivered to the load can be doubled by using the bridge connection shown here. Output clamping to the supplies can be provided by using a bridge-rectifier assembly.

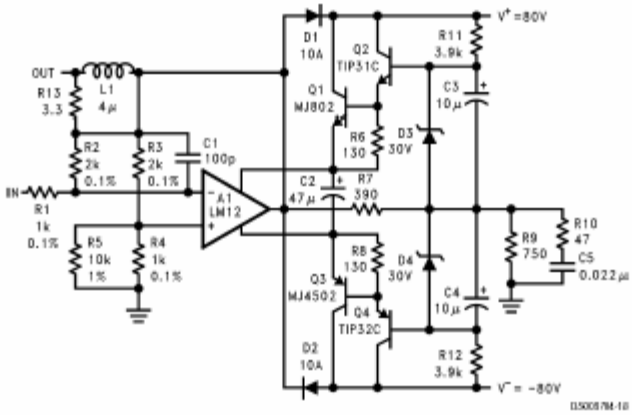
## Application Information (Continued)




One limitation of the standard bridge connection is that the load cannot be returned to ground. This can be circumvented by operating the bridge with floating supplies, as shown above. For single-ended drive, either input can be grounded.



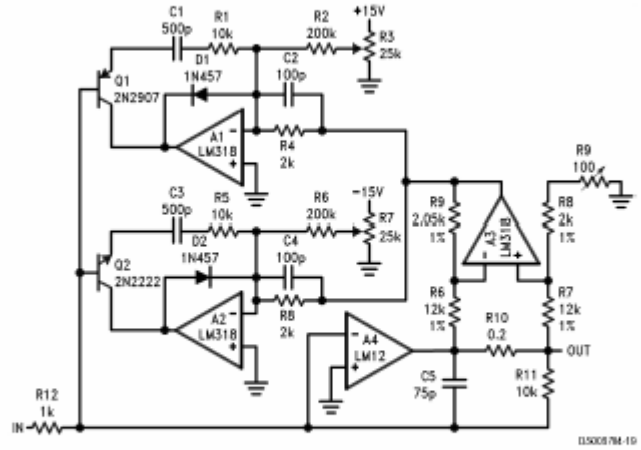

This circuit shows how two amplifiers can be cascaded to double output swing. The advantage over the bridge is that the output can be increased with any number of stages, although separate supplies are required for each.




Discrete transistors can be used to increase output drive to ±70V at ±10A as shown above. With proper thermal design, the IC will provide safe-area protection for the external transistors. Voltage gain is about thirty.

## Application Information (Continued)

OPERATIONAL POWER SUPPLY

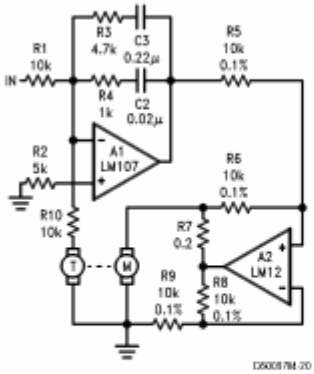



**Note:** Supply voltages for the LM318s are ±15V

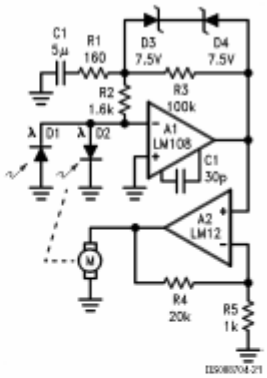
External current limit can be provided for a power op amp as shown above. The positive and negative current limits can be set precisely and independently. Fast response is assured by $D_1$ and $D_2$. Adjustment range can be set down to zero with potentiometers $R_3$ and $R_7$. Alternately, the limit can be programmed from a voltage supplied to $R_2$ and $R_6$. This is the set up required for an operational power supply or voltage-programmable power source.

SERVO AMPLIFIERS

When making servo systems with a power op amp, there is a temptation to use it for frequency shaping to stabilize the servo loop. Sometimes this works; other times there are better ways; and occasionally it just doesn't fly. Usually it's a matter of how quickly and to what accuracy the servo must stabilize.



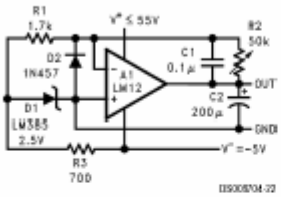

This motor/tachometer servo gives an output speed proportional to input voltage. A low-level op amp is used for frequency shaping while the power op amp provides current drive to the motor. Current drive eliminates loop phase shift due to motor inductance and makes high-performance servos easier to stabilize.



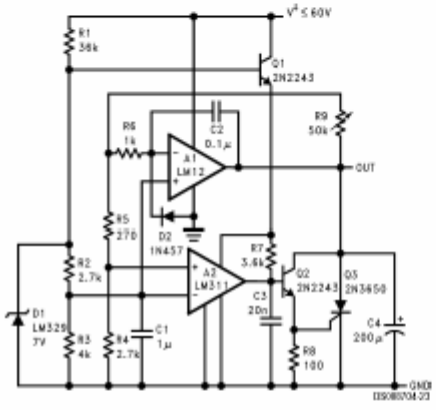

This position servo uses an op amp to develop the rate signal electrically instead of using a tachometer. In high-performance servos, rate signals must be developed with large error signals well beyond saturation of the motor drive. Using a separate op amp with a feedback clamp allows the rate signal to be developed properly with position errors more than an order of magnitude beyond the loop-saturation level as long as the photodiode sensors are positioned with this in mind.

## Application Information (Continued)

VOLTAGE REGULATORS

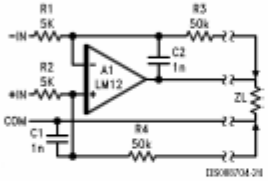



An op amp can be used as a positive or negative regulator. Unlike most regulators, it can sink current to absorb energy dumped back into the output. This positive regulator has a 0–50V output range.



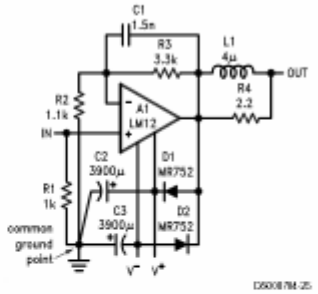

Dual supplies are not required to use an op amp as a voltage regulator if zero output is not required. This 4V to 50V regulator operates from a single supply. Should the op amp not be able to absorb enough energy to control an overvoltage condition, a SCR will crowbar the output.

REMOTE SENSING




Remote sensing as shown above allows the op amp to correct for dc drops in cables connecting the load. Even so, cable drop will affect transient response. Degradation can be minimized by using twisted, heavy-gauge wires on the output line. Normally, common and one input are connected together at the sending end.

AUDIO AMPLIFIERS




A power amplifier suitable for use in high-quality audio equipment is shown above. Harmonic distortion is about 0.01-percent. Intermodulation distortion (60 Hz/7 kHz, 4:1) measured 0.015-percent. Transient response and saturation recovery are clean, and the 9 V/µs slew rate of the LM12 virtually eliminates transient intermodulation distortion. Using separate amplifiers to drive low- and high-frequency speakers gets rid of high-level crossover networks and attenuators. Further, it prevents clipping on the low-frequency channel from distorting the high frequencies.

DETERMINING MAXIMUM DISSIPATION

It is a simple matter to establish power requirements for an op amp driving a resistive load at frequencies well below 10 Hz. Maximum dissipation occurs when the output is at one-half the supply voltage with high-line conditions. The individual output transistors must be rated to handle this power continuously at the maximum expected case temperature. The power rating is limited by the maximum junction temperature as determined by

$$T_J = T_C + P_{DISS}\,\theta_{JC},$$

where $T_C$ is the case temperature as measured at the center of the package bottom, $P_{DISS}$ is the maximum power dissipation and $\theta_{JC}$ is the thermal resistance at the operating voltage of the output transistor. Recommended maximum junction temperatures are 200˚C within the power transistor and 150˚C for the control circuitry.

If there is ripple on the supply bus, it is valid to use the average value in worst-case calculations as long as the peak rating of the power transistor is not exceeded at the ripple peak. With 120 Hz ripple, this is 1.5 times the continuous power rating.

Dissipation requirements are not so easily established with time varying output signals, especially with reactive loads. Both peak and continuous dissipation ratings must be taken into account, and these depend on the signal waveform as well as load characteristics.

With a sine wave output, analysis is fairly straightforward. With supply voltages of $\pm V_S$, the maximum average power dissipation of both output transistors is

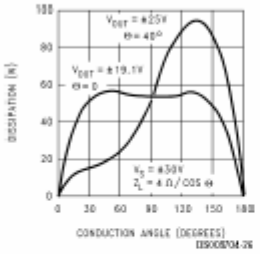
$$P_{MAX} = \frac{2V_S^2}{\pi^2 Z_L \cos\theta}, \quad \theta < 40°;$$

and

$$P_{MAX} = \frac{V_S^2}{2Z_L}\left[\frac{4}{\pi} - \cos\theta\right], \quad \theta \geq 40°,$$

## Application Information (Continued)

where $Z_L$ is the magnitude of the load impedance and $\theta$ its phase angle. Maximum average dissipation occurs below maximum output swing for $\theta < 40^\circ$.




The instantaneous power dissipation over the conducting half cycle of one output transistor is shown here. Power dissipation is near zero on the other half cycle. The output level is that resulting in maximum peak and average dissipation. Plots are given for a resistive and a series RL load. The latter is representative of a 4Ω loudspeaker operating below resonance and would be the worst case condition in most audio applications. The peak dissipation of each transistor is about four times average. In ac applications, power capability is often limited by the peak ratings of the power transistor.

The pulse thermal resistance of the LM12 is specified for constant power pulse duration. Establishing an exact equivalency between constant-power pulses and those encountered in practice is not easy. However, for sine waves, reasonable estimates can be made at any frequency by assuming a constant power pulse amplitude given by:

$$P_{PK} \cong \frac{V_S^2}{2Z_L}\left[1-\cos(\phi-\theta)\right],$$

where $\phi = 60^\circ$ and $\theta$ is the absolute value of the phase angle of $Z_L$. Equivalent pulse width is $t_{ON} \cong 0.4\tau$ for $\theta = 0$ and $t_{ON} \cong 0.2\tau$ for $\theta \geq 20^\circ$, where $\tau$ is the period of the output waveform.

### DISSIPATION DRIVING MOTORS

A motor with a locked rotor looks like an inductance in series with a resistance, for purposes of determining driver dissipation. With slow-response servos, the maximum signal amplitude at frequencies where motor inductance is significant can be so small that motor inductance does not have to be taken into account. If this is the case, the motor can be treated as a simple, resistive load as long as the rotor speed is low enough that the back emf is small by comparison to the supply voltage of the driver transistor.

A permanent-magnet motor can build up a back emf that is equal to the output swing of the op amp driving it. Reversing this motor from full speed requires the output drive transistor to operate, initially, along a loadline based upon the motor resistance and total supply voltage. Worst case, this loadline will have to be within the continuous dissipation rating of the drive transistor; but system dynamics may permit taking advantage of the higher pulse ratings. Motor inductance can cause added stress if system response is fast.

Shunt- and series-wound motors can generate back emf's that are considerably more than the total supply voltage, resulting in even higher peak dissipation than a permanent-magnet motor having the same locked-rotor resistance.

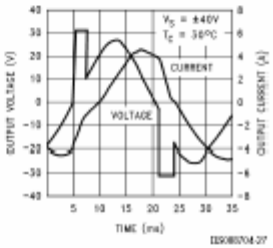
### VOLTAGE REGULATOR DISSIPATION

The pass transistor dissipation of a voltage regulator is easily determined in the operating mode. Maximum continuous dissipation occurs with high line voltage and maximum load current. As discussed earlier, ripple voltage can be averaged if peak ratings are not exceeded; however, a higher average voltage will be required to insure that the pass transistor does not saturate at the ripple minimum.

Conditions during start-up can be more complex. If the input voltage increases slowly such that the regulator does not go into current limit charging output capacitance, there are no problems. If not, load capacitance and load characteristics must be taken into account. This is also the case if automatic restart is required in recovering from overloads.

Automatic restart or start-up with fast-rising input voltages cannot be guaranteed unless the continuous dissipation rating of the pass transistor is adequate to supply the load current continuously at all voltages below the regulated output voltage. In this regard, the LM12 performs much better than IC regulators using foldback current limit, especially with high-line input voltage above 20V.

### POWER LIMITING




Should the power ratings of the LM12 be exceeded, dynamic safe-area protection is activated. Waveforms with this power limiting are shown for the LM12 driving ±26V at 30 Hz into 3Ω in series with 24 mH ($\theta = 45^\circ$). With an inductive load, the output clamps to the supplies in power limit, as above. With resistive loads, the output voltage drops in limit. Behavior with more complex RCL loads is between these extremes.

Secondary thermal limit is activated should the case temperature exceed 150°C. This thermal limit shuts down the IC completely (open output) until the case temperature drops to about 145°C. Recovery may take several seconds.

### POWER SUPPLIES

Power op amps do not require regulated supplies. However, the worst-case output power is determined by the low-line supply voltage in the ripple trough. The worst-case power dissipation is established by the average supply voltage with high-line conditions. The loss in power output that can be guaranteed is the square of the ratio of these two voltages.

Relatively simple off-line switching power supplies can provide voltage conversion, line isolation and 5-percent regulation while reducing size and weight.

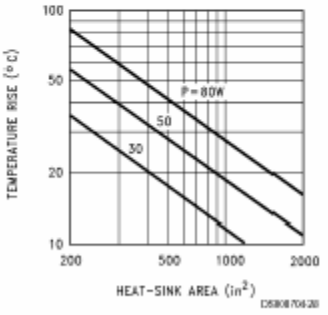
The regulation against ripple and line variations can provide a substantial increase in the power output that can be guar-

## Application Information (Continued)

anteed under worst-case conditions. In addition, switching power supplies can convert low-voltage power sources such as automotive batteries up to regulated, dual, high-voltage supplies optimized for powering power op amps.

### HEAT SINKING

A semiconductor manufacturer has no control over heat sink design. Temperature rating can only be based upon case temperature as measured at the center of the package bottom. With power pulses of longer duration than 100 ms, case temperature is almost entirely dependent on heat sink design and the mounting of the IC to the heat sink.




The design of heat sink is beyond the scope of this work. Convection-cooled heat sinks are available commercially, and their manufacturers should be consulted for ratings. The preceding figure is a rough guide for temperature rise as a function of fin area (both sides) available for convection cooling.

Proper mounting of the IC is required to minimize the thermal drop between the package and the heat sink. The heat sink must also have enough metal under the package to conduct heat from the center of the package bottom to the fins without excessive temperature drop.

A thermal grease such as Wakefield type 120 or Thermalloy Thermacote should be used when mounting the package to the heat sink. Without this compound, thermal resistance will be no better than 0.5˚C/W, and probably much worse. With the compound, thermal resistance will be 0.2˚C/W or less, assuming under 0.005 inch combined flatness runout for the package and heat sink. Proper torquing of the mounting bolts is important. Four to six inch-pounds is recommended.

Should it be necessary to isolate V− from the heat sink, an insulating washer is required. Hard washers like beryllium oxide, anodized aluminum and mica require the use of thermal compound on both faces. Two-mil mica washers are most common, giving about 0.4˚C/W interface resistance with the compound. Silicone-rubber washers are also available. A 0.5˚C/W thermal resistance is claimed without thermal compound. Experience has shown that these rubber washers deteriorate and must be replaced should the IC be dismounted.

"Isostrate" insulating pads for four-lead TO-3 packages are available from Power Devices, Inc. Thermal grease is not required, and the insulators should not be reused.

## Definition of Terms

Input offset voltage: The absolute value of the voltage between the input terminals with the output voltage and current at zero.

Input bias current: The absolute value of the average of the two input currents with the output voltage and current at zero.

Input offset current: The absolute value of the difference in the two input currents with the output voltage and current at zero.

Common-mode rejection: The ratio of the input voltage range to the change in offset voltage between the extremes.

Supply-voltage rejection: The ratio of the specified supply-voltage change to the change in offset voltage between the extremes.

Output saturation threshold: The output swing limit for a specified input drive beyond that required for zero output. It is measured with respect to the supply to which the output is swinging.

Large signal voltage gain: The ratio of the output voltage swing to the differential input voltage required to drive the output from zero to either swing limit. The output swing limit is the supply voltage less a specified quasi-saturation voltage. A pulse of short enough duration to minimize thermal effects is used as a measurement signal.

Thermal gradient feedback: The input offset voltage change caused by thermal gradients generated by heating of the output transistors, but not the package. This effect is delayed by several milliseconds and results in increased gain error below 100 Hz.

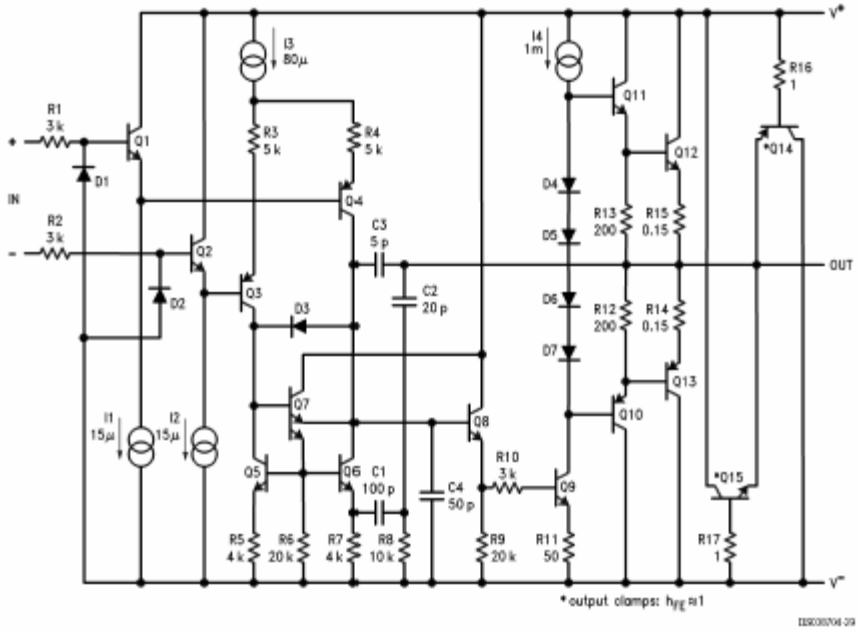
Output-current limit: The output current with a fixed output voltage and a large input overdrive. The limiting current drops with time once the protection circuitry is activated.

Power dissipation rating: The power that can be dissipated for a specified time interval without activating the protection circuitry. For time intervals in excess of 100 ms, dissipation capability is determined by heat sinking of the IC package rather than by the IC itself.

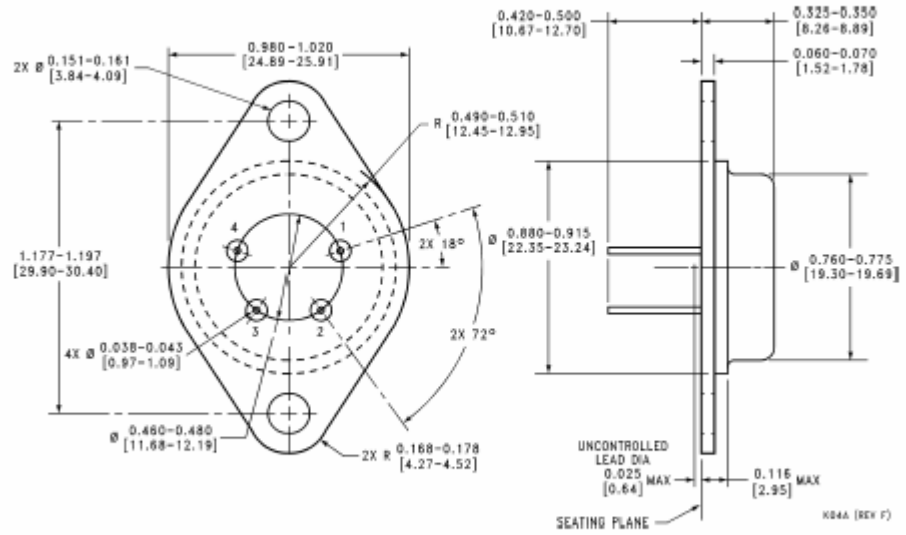
Thermal resistance: The peak, junction-temperature rise, per unit of internal power dissipation, above the case temperature as measured at the center of the package bottom. The dc thermal resistance applies when one output transistor is operating continuously. The ac thermal resistance applies with the output transistors conducting alternately at a high enough frequency that the peak capability of neither transistor is exceeded.

Supply current: The current required from the power source to operate the amplifier with the output voltage and current at zero.

## Equivalent Schematic (excluding active protection circuitry)



## Physical Dimensions inches (millimeters) unless otherwise noted




4-Lead TO-3 Steel Package (K)
Order Number LM12CLK
NS Package Number K04A

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## B. INTERNATIONAL RECTIFIER IRG4PH5OKD IGBT [From Ref. 13.]

International
IOR Rectifier

PD- 91575B

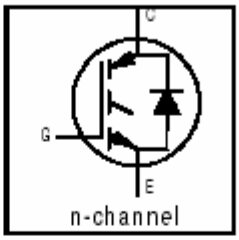
# IRG4PH50KD

INSULATED GATE BIPOLAR TRANSISTOR WITH ULTRAFAST SOFT RECOVERY DIODE

Short Circuit Rated
UltraFast IGBT

### Features

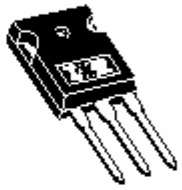
- High short circuit rating optimized for motor control, $t_{sc}$ =10µs, $V_{CC}$ = 720V , $T_J$ = 125°C, $V_{GE}$ = 15V
- Combines low conduction losses with high switching speed
- Tighter parameter distribution and higher efficiency than previous generations
- IGBT co-packaged with HEXFRED™ ultrafast, ultrasoft recovery antiparallel diodes




$V_{CES}$ = 1200V

$V_{CE(on)\ typ.}$ = 2.77V

@$V_{GE}$ = 15V, $I_C$ = 24A



TO-247AC

### Benefits

- Latest generation 4 IGBT's offer highest power density motor controls possible
- HEXFRED™ diodes optimized for performance with IGBTs. Minimized recovery characteristics reduce noise, EMI and switching losses
- This part replaces the IRGPH50KD2 and IRGPH50MD2 products
- For hints see design tip 97003

### Absolute Maximum Ratings

| | Parameter | Max. | Units |
|---|---|---|---|
| $V_{CES}$ | Collector-to-Emitter Voltage | 1200 | V |
| $I_C$ @ $T_C$ = 25°C | Continuous Collector Current | 45 | A |
| $I_C$ @ $T_C$ = 100°C | Continuous Collector Current | 24 | |
| $I_{CM}$ | Pulsed Collector Current ① | 90 | |
| $I_{LM}$ | Clamped Inductive Load Current ② | 90 | |
| $I_F$ @ $T_C$ = 100°C | Diode Continuous Forward Current | 16 | |
| $I_{FM}$ | Diode Maximum Forward Current | 90 | |
| $t_{sc}$ | Short Circuit Withstand Time | 10 | µs |
| $V_{GE}$ | Gate-to-Emitter Voltage | ± 20 | V |
| $P_D$ @ $T_C$ = 25°C | Maximum Power Dissipation | 200 | W |
| $P_D$ @ $T_C$ = 100°C | Maximum Power Dissipation | 78 | |
| $T_J$<br>$T_{STG}$ | Operating Junction and<br>Storage Temperature Range | -55 to +150 | °C |
| | Soldering Temperature, for 10 sec. | 300 (0.063 in. (1.6mm) from case) | |
| | Mounting Torque, 6-32 or M3 Screw. | 10 lbf•in (1.1 N•m) | |

### Thermal Resistance

| | Parameter | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| $R_{\theta JC}$ | Junction-to-Case - IGBT | — | — | 0.64 | °C/W |
| $R_{\theta JC}$ | Junction-to-Case - Diode | — | — | 0.83 | |
| $R_{\theta CS}$ | Case-to-Sink, flat, greased surface | — | 0.24 | — | |
| $R_{\theta JA}$ | Junction-to-Ambient, typical socket mount | — | — | 40 | |
| Wt | Weight | — | 6 (0.21) | — | g (oz) |

## Electrical Characteristics @ $T_J$ = 25°C (unless otherwise specified)

| | Parameter | Min. | Typ. | Max. | Units | Conditions |
|---|---|---|---|---|---|---|
| $V_{(BR)CES}$ | Collector-to-Emitter Breakdown Voltage③ | 1200 | — | — | V | $V_{GE}$ = 0V, $I_C$ = 250µA |
| $\Delta V_{(BR)CES}/\Delta T_J$ | Temperature Coeff. of Breakdown Voltage | — | 0.91 | — | V/°C | $V_{GE}$ = 0V, $I_C$ = 1.0mA |
| $V_{CE(on)}$ | Collector-to-Emitter Saturation Voltage | — | 2.77 | 3.5 | V | $I_C$ = 24A $V_{GE}$ = 15V |
| | | — | 3.28 | — | | $I_C$ = 45A See Fig. 2, 5 |
| | | — | 2.54 | — | | $I_C$ = 24A, $T_J$ = 150°C |
| $V_{GE(th)}$ | Gate Threshold Voltage | 3.0 | — | 6.0 | | $V_{CE}$ = $V_{GE}$, $I_C$ = 250µA |
| $\Delta V_{GE(th)}/\Delta T_J$ | Temperature Coeff. of Threshold Voltage | — | -10 | — | mV/°C | $V_{CE}$ = $V_{GE}$, $I_C$ = 250µA |
| $g_{fe}$ | Forward Transconductance ④ | 13 | 19 | — | S | $V_{CE}$ = 100V, $I_C$ = 24A |
| $I_{CES}$ | Zero Gate Voltage Collector Current | — | — | 250 | µA | $V_{GE}$ = 0V, $V_{CE}$ = 1200V |
| | | — | — | 6500 | | $V_{GE}$ = 0V, $V_{CE}$ = 1200V, $T_J$ = 150°C |
| $V_{FM}$ | Diode Forward Voltage Drop | — | 2.5 | 3.5 | V | $I_C$ = 16A See Fig. 13 |
| | | — | 2.1 | 3.0 | | $I_C$ = 16A, $T_J$ = 150°C |
| $I_{GES}$ | Gate-to-Emitter Leakage Current | — | — | ±100 | nA | $V_{GE}$ = ±20V |

## Switching Characteristics @ $T_J$ = 25°C (unless otherwise specified)

| | Parameter | Min. | Typ. | Max. | Units | Conditions |
|---|---|---|---|---|---|---|
| $Q_g$ | Total Gate Charge (turn-on) | — | 180 | 270 | nC | $I_C$ = 24A |
| $Q_{ge}$ | Gate - Emitter Charge (turn-on) | — | 25 | 38 | | $V_{CC}$ = 400V See Fig.8 |
| $Q_{gc}$ | Gate - Collector Charge (turn-on) | — | 70 | 110 | | $V_{GE}$ = 15V |
| $t_{d(on)}$ | Turn-On Delay Time | — | 87 | — | ns | |
| $t_r$ | Rise Time | — | 100 | — | | $T_J$ = 25°C |
| $t_{d(off)}$ | Turn-Off Delay Time | — | 140 | 300 | | $I_C$ = 24A, $V_{CC}$ = 800V |
| $t_f$ | Fall Time | — | 200 | 300 | | $V_{GE}$ = 15V, $R_G$ = 5.0Ω |
| $E_{on}$ | Turn-On Switching Loss | — | 3.83 | — | mJ | Energy losses include "tail" |
| $E_{off}$ | Turn-Off Switching Loss | — | 1.90 | — | | and diode reverse recovery |
| $E_{ts}$ | Total Switching Loss | — | 5.73 | 7.9 | | See Fig. 9,10,18 |
| $t_{sc}$ | Short Circuit Withstand Time | 10 | — | — | µs | $V_{CC}$ = 720V, $T_J$ = 125°C |
| | | | | | | $V_{GE}$ = 15V, $R_G$ = 5.0Ω |
| $t_{d(on)}$ | Turn-On Delay Time | — | 67 | — | ns | $T_J$ = 150°C, See Fig. 10,11,18 |
| $t_r$ | Rise Time | — | 72 | — | | $I_C$ = 24A, $V_{CC}$ = 800V |
| $t_{d(off)}$ | Turn-Off Delay Time | — | 310 | — | | $V_{GE}$ = 15V, $R_G$ = 5.0Ω, |
| $t_f$ | Fall Time | — | 390 | — | | Energy losses include "tail" |
| $E_{ts}$ | Total Switching Loss | — | 8.36 | — | mJ | and diode reverse recovery |
| $L_E$ | Internal Emitter Inductance | — | 13 | — | nH | Measured 5mm from package |
| $C_{ies}$ | Input Capacitance | — | 2800 | — | pF | $V_{GE}$ = 0V |
| $C_{oes}$ | Output Capacitance | — | 140 | — | | $V_{CC}$ = 30V See Fig. 7 |
| $C_{res}$ | Reverse Transfer Capacitance | — | 53 | — | | $f$ = 1.0MHz |
| $t_{rr}$ | Diode Reverse Recovery Time | — | 90 | 135 | ns | $T_J$ = 25°C See Fig. |
| | | — | 164 | 245 | | $T_J$ = 125°C 14 $I_F$ = 16A |
| $I_{rr}$ | Diode Peak Reverse Recovery Current | — | 5.8 | 10 | A | $T_J$ = 25°C See Fig. |
| | | — | 8.3 | 15 | | $T_J$ = 125°C 15 $V_R$ = 200V |
| $Q_{rr}$ | Diode Reverse Recovery Charge | — | 260 | 675 | nC | $T_J$ = 25°C See Fig. |
| | | — | 680 | 1838 | | $T_J$ = 125°C 16 di/dt = 200A/µs |
| $di_{(rec)M}/dt$ | Diode Peak Rate of Fall of Recovery | — | 120 | — | A/µs | $T_J$ = 25°C See Fig. |
| | During $t_b$ | — | 76 | — | | $T_J$ = 125°C 17 |

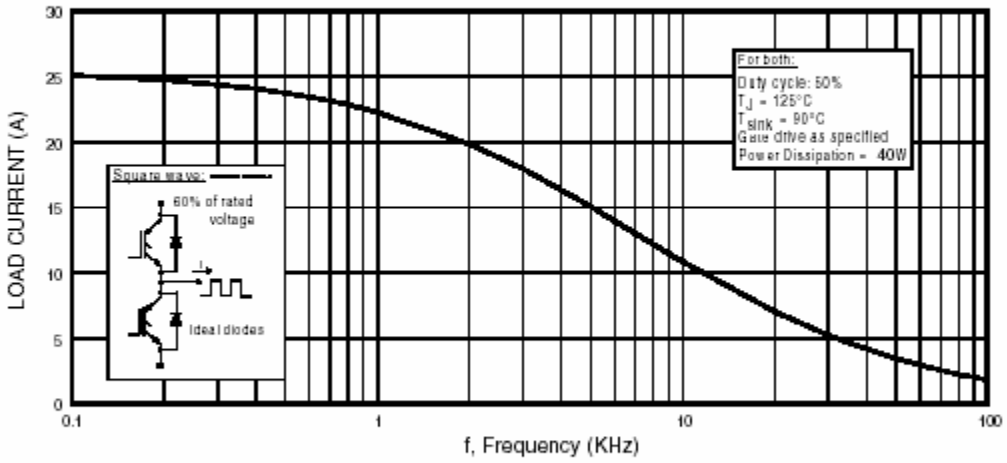



**Fig. 1** - Typical Load Current vs. Frequency
(Load Current = $I_{RMS}$ of fundamental)

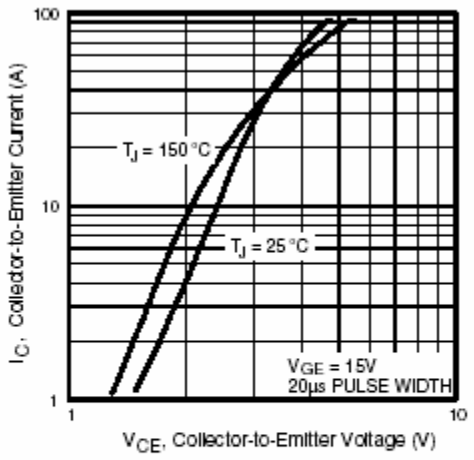



**Fig. 2** - Typical Output Characteristics

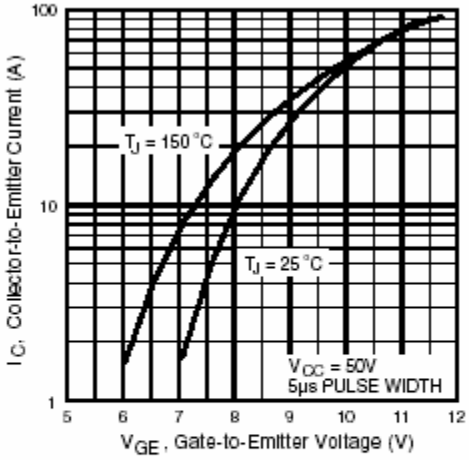



**Fig. 3** - Typical Transfer Characteristics

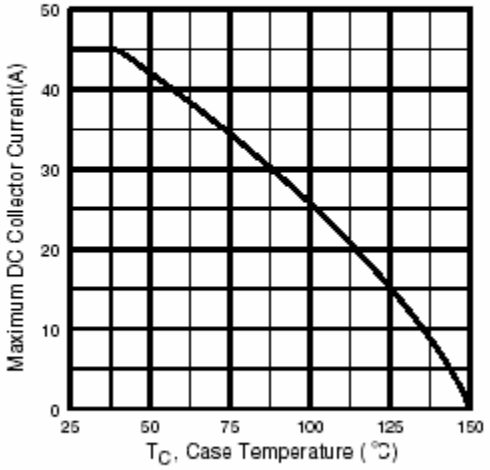



Fig. 4 - Maximum Collector Current vs. Case Temperature

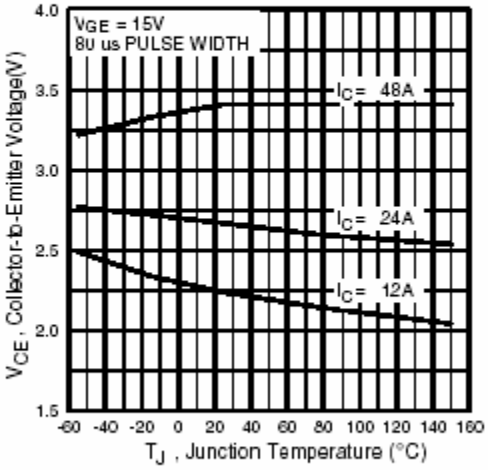



Fig. 5 - Typical Collector-to-Emitter Voltage vs. Junction Temperature

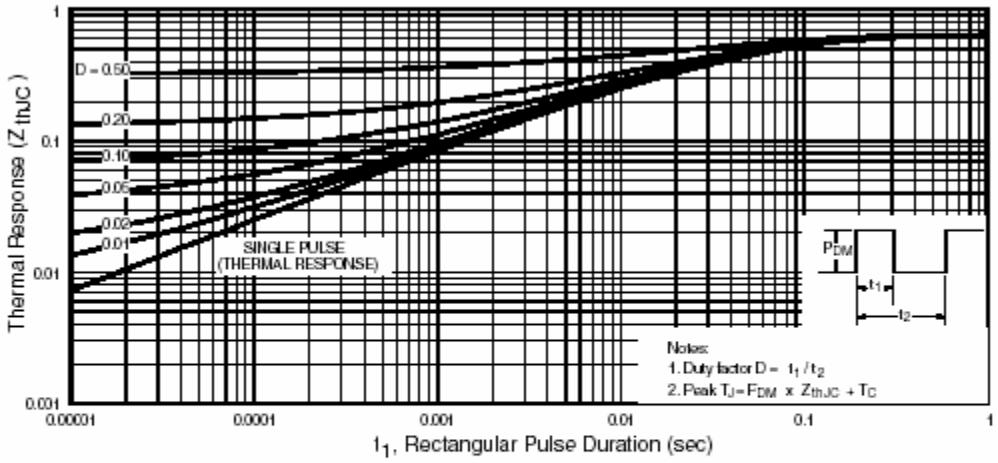



Fig. 6 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

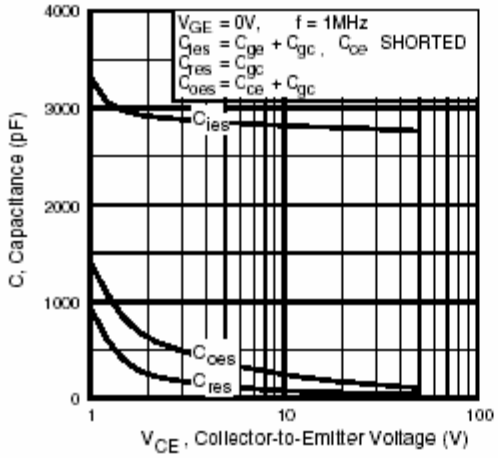



Fig. 7 - Typical Capacitance vs. Collector-to-Emitter Voltage

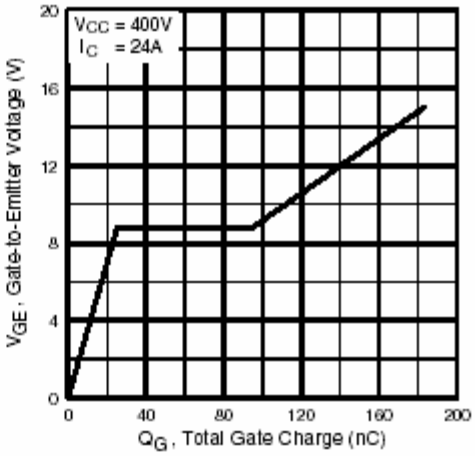



Fig. 8 - Typical Gate Charge vs. Gate-to-Emitter Voltage

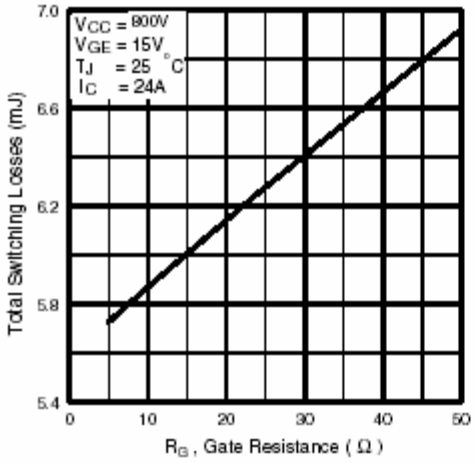



Fig. 9 - Typical Switching Losses vs. Gate Resistance

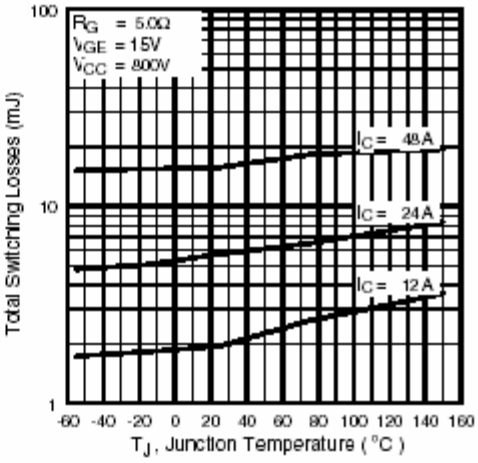



Fig. 10 - Typical Switching Losses vs. Junction Temperature

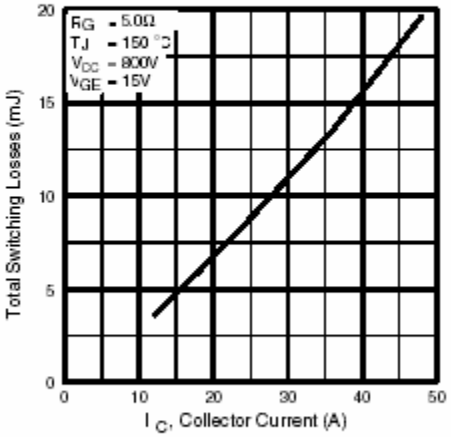



Fig. 11 - Typical Switching Losses vs. Collector Current

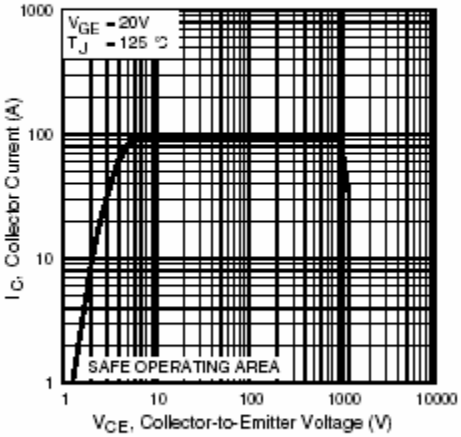



Fig. 12 - Turn-Off SOA

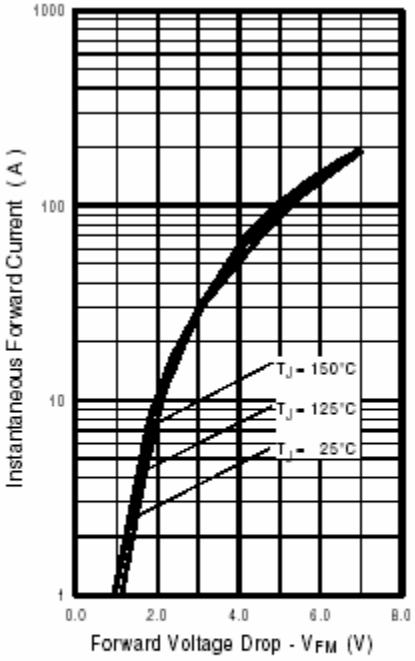



Fig. 13 - Typical Forward Voltage Drop vs. Instantaneous Forward Current

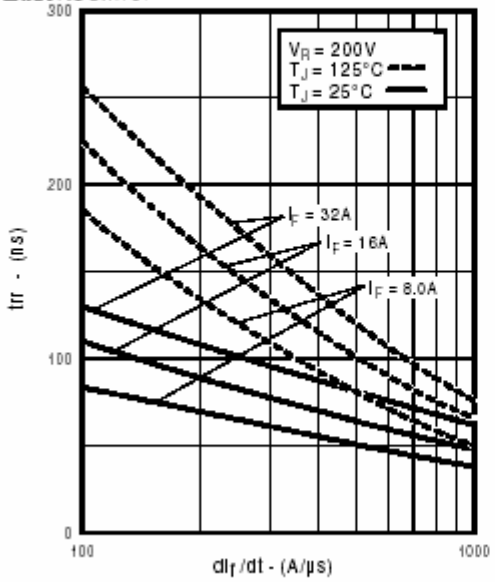



Fig. 14 - Typical Reverse Recovery vs. $di_f/dt$

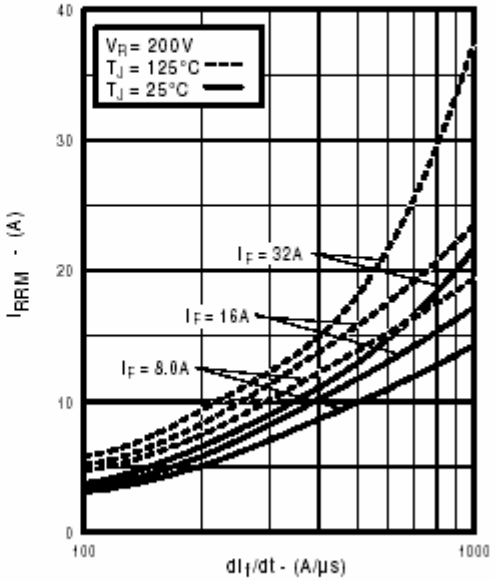



Fig. 15 - Typical Recovery Current vs. $di_f/dt$

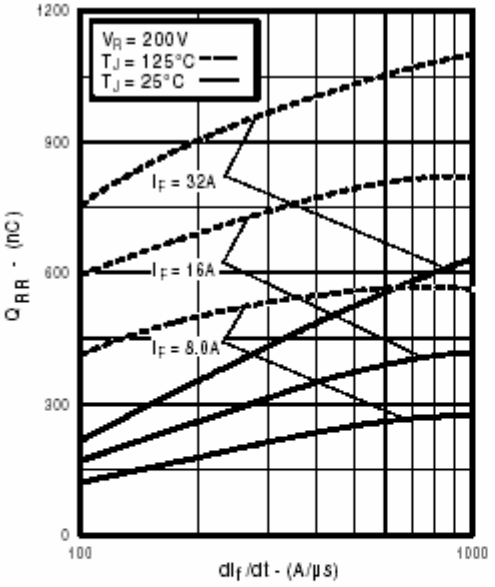



Fig. 16 - Typical Stored Charge vs. $di_f/dt$

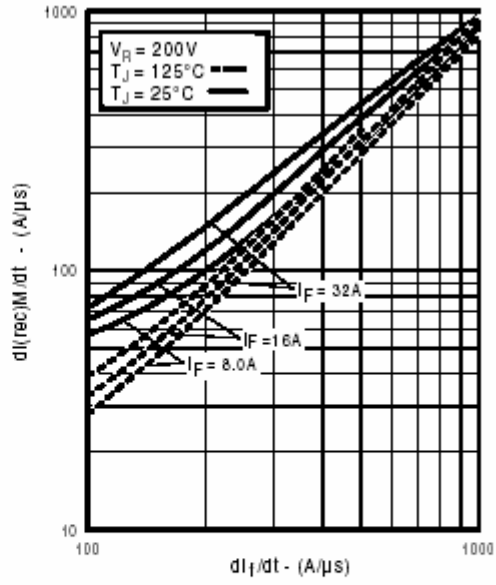



Fig. 17 - Typical $di_{(rec)M}/dt$ vs. $di_f/dt$

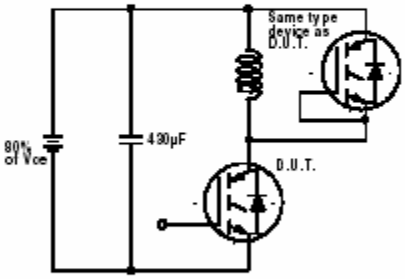



Fig. 18a - Test Circuit for Measurement of $I_{LM}$, $E_{on}$, $E_{off(diode)}$, $t_{rr}$, $Q_{rr}$, $I_{rr}$, $t_{d(on)}$, $t_r$, $t_{d(off)}$, $t_f$

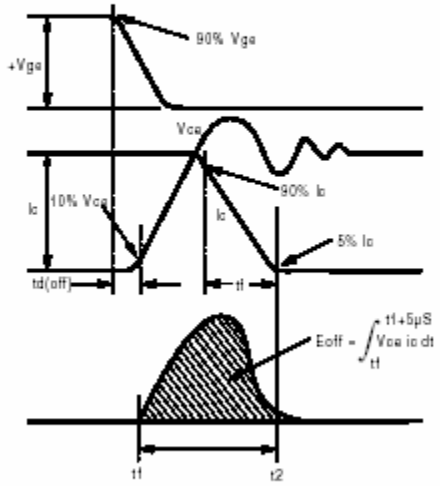



Fig. 18b - Test Waveforms for Circuit of Fig. 18a, Defining $E_{off}$, $t_{d(off)}$, $t_f$

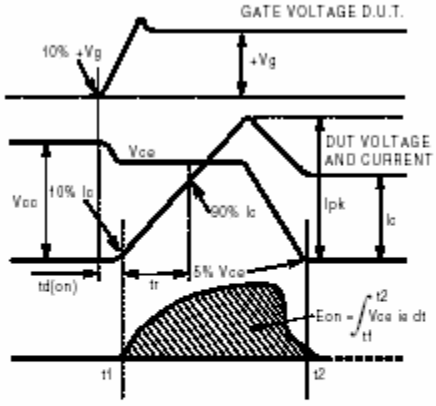



Fig. 18c - Test Waveforms for Circuit of Fig. 18a, Defining $E_{on}$, $t_{d(on)}$, $t_r$

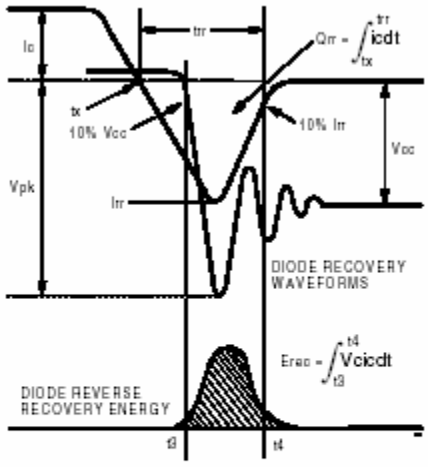



Fig. 18d - Test Waveforms for Circuit of Fig. 18a, Defining $E_{rec}$, $t_{rr}$, $Q_{rr}$, $I_{rr}$

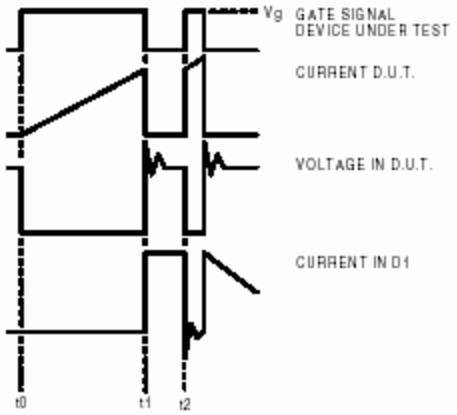



Figure 18e. Macro Waveforms for Figure 18a's Test Circuit

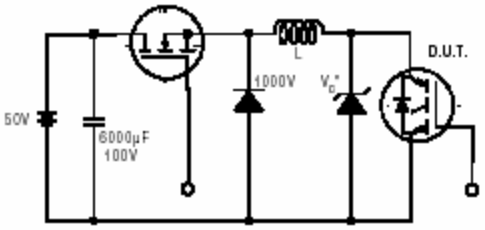



Figure 19. Clamped Inductive Load Test Circuit

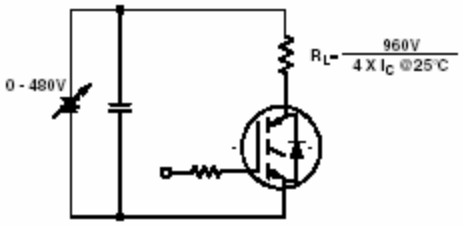



Figure 20. Pulsed Collector Current Test Circuit

## Notes:

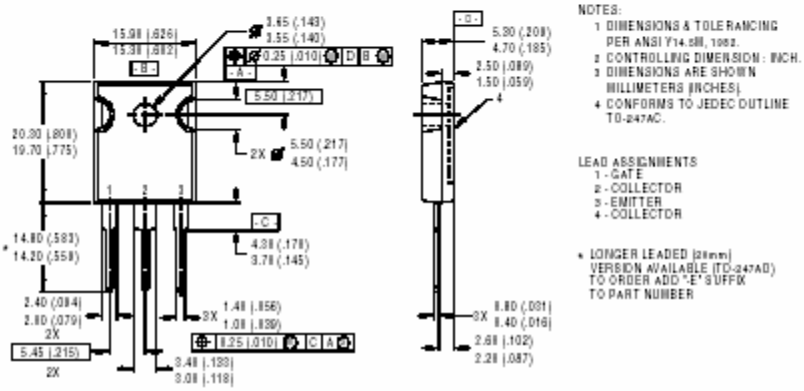
① Repetitive rating: $V_{GE}$=20V; pulse width limited by maximum junction temperature (figure 20)

② $V_{CC}$=80%($V_{CES}$), $V_{GE}$=20V, L=10µH, $R_G$=5.0Ω (figure 19)

③ Pulse width ≤ 80µs; duty factor ≤ 0.1%.

④ Pulse width 5.0µs, single shot.

## Case Outline — TO-247AC




**CONFORMS TO JEDEC OUTLINE TO-247AC (TO-3P)**
Dimensions in Millimeters and (Inches)

International
IOR Rectifier

IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105
IR EUROPEAN REGIONAL CENTRE: 439/445 Godstone Rd, Whyteleafe, Surrey CR3 0BL, UK Tel: ++ 44 (0)20 8645 8000
IR CANADA: 15 Lincoln Court, Brampton, Ontario L6T3Z2, Tel: (905) 453 2200
IR GERMANY: Saalburgstrasse 157, 61350 Bad Homburg Tel: ++ 49 (0) 6172 96590
IR ITALY: Via Liguria 49, 10071 Borgaro, Torino Tel: ++ 39 011 451 0111
IR JAPAN: K&H Bldg., 2F, 30-4 Nishi-Ikebukuro 3-Chome, Toshima-Ku, Tokyo 171 Tel: 81 (0)3 3983 0086
IR SOUTHEAST ASIA: 1 Kim Seng Promenade, Great World City West Tower, 13-11, Singapore 237994 Tel: ++ 65 (0)838 4630
IR TAIWAN: 16 Fl. Suite D. 207, Sec. 2, Tun Haw South Road, Taipei, 10673 Tel: 886-(0)2 2377 9936
*Data and specifications subject to change without notice. 7/00*

## C. INTERNATIONAL RECTIFIER HFA25PB60 HEXFRED™ DIODE [From Ref. 14.]

Bulletin PD-2.338 rev. A 11/00

International
IOR Rectifier

# HFA25PB60

HEXFRED™

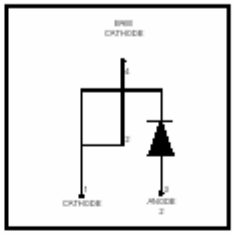
Ultrafast, Soft Recovery Diode

### Features

- Ultrafast Recovery
- Ultrasoft Recovery
- Very Low $I_{RRM}$
- Very Low $Q_{rr}$
- Specified at Operating Conditions

### Benefits

- Reduced RFI and EMI
- Reduced Power Loss in Diode and Switching Transistor
- Higher Frequency Operation
- Reduced Snubbing
- Reduced Parts Count




$V_R$ = 600V
$V_F$(typ.)* = 1.3V
$I_{F(AV)}$ = 25A
$Q_{rr}$ (typ.)= 112nC
$I_{RRM}$ = 10A
$t_{rr}$(typ.) = 23ns
$di_{(rec)M}/dt$ (typ.) = 250A/µs

TO-247AC (Modified)

### Description

International Rectifier's HFA25PB60 is a state of the art ultra fast recovery diode. Employing the latest in epitaxial construction and advanced processing techniques it features a superb combination of characteristics which result in performance which is unsurpassed by any rectifier previously available. With basic ratings of 600 volts and 25 amps continuous current, the HFA25PB60 is especially well suited for use as the companion diode for IGBTs and MOSFETs. In addition to ultra fast recovery time, the HEXFRED product line features extremely low values of peak recovery current ($I_{RRM}$) and does not exhibit any tendency to "snap-off" during the $t_b$ portion of recovery. The HEXFRED features combine to offer designers a rectifier with lower noise and significantly lower switching losses in both the diode and the switching transistor. These HEXFRED advantages can help to significantly reduce snubbing, component count and heatsink sizes. The HEXFRED HFA25PB60 is ideally suited for applications in power supplies and power conversion systems (such as inverters), motor drives, and many other similar applications where high speed, high efficiency is needed.

### Absolute Maximum Ratings

| | Parameter | Max | Units |
|---|---|---|---|
| $V_R$ | Cathode-to-Anode Voltage | 600 | V |
| $I_F$ @ $T_C$ = 25°C | Continuous Forward Current | | A |
| $I_F$ @ $T_C$ = 100°C | Continuous Forward Current | 25 | |
| $I_{FSM}$ | Single Pulse Forward Current | 225 | |
| $I_{FRM}$ | Maximum Repetitive Forward Current | 100 | |
| $P_D$ @ $T_C$ = 25°C | Maximum Power Dissipation | 151 | W |
| $P_D$ @ $T_C$ = 100°C | Maximum Power Dissipation | 60 | |
| $T_J$ | Operating Junction and | -55 to +150 | C |
| $T_{STG}$ | Storage Temperature Range | | |

* 125°C

1

## Electrical Characteristics @ $T_J$ = 25°C (unless otherwise specified)

| | Parameter | Min | Typ | Max | Units | Test Conditions |
|---|---|---|---|---|---|---|
| $V_{BR}$ | Cathode Anode Breakdown Voltage | 600 | ---- | ---- | V | $I_R$ = 100µA |
| $V_{FM}$ | Max Forward Voltage | ---- | 1.3 | 1.7 | V | $I_F$ = 25A |
| | | ---- | 1.5 | 2.0 | | $I_F$ = 50A See Fig. 1 |
| | | ---- | 1.3 | 1.7 | | $I_F$ = 25A, $T_J$ = 125°C |
| $I_{RM}$ | Max Reverse Leakage Current | ---- | 1.5 | 20 | µA | $V_R$ = $V_R$ Rated See Fig. 2 |
| | | ---- | 600 | 2000 | | $T_J$ = 125°C, $V_R$ = 0.8 x $V_R$ Rated |
| $C_T$ | Junction Capacitance | ---- | 55 | 100 | pF | $V_R$ = 200V See Fig. 3 |
| $L_S$ | Series Inductance | ---- | 12 | ---- | nH | Measured lead to lead 5mm from package body |

## Dynamic Recovery Characteristics @ $T_J$ = 25°C (unless otherwise specified)

| | Parameter | Min | Typ | Max | Units | Test Conditions | |
|---|---|---|---|---|---|---|---|
| $t_{rr}$ | Reverse Recovery Time | ---- | 23 | ---- | ns | $I_F$ = 1.0A, di/dt = 200A/µs, $V_R$ = 30V | |
| $t_{rr1}$ | See Fig. 5, 6 & 16 | ---- | 50 | 75 | | $T_J$ = 25°C | $I_F$ = 25A |
| $t_{rr2}$ | | ---- | 105 | 160 | | $T_J$ = 125°C | |
| $I_{RRM1}$ | Peak Recovery Current | ---- | 4.5 | 10 | A | $T_J$ = 25°C | $V_R$ = 200V |
| $I_{RRM2}$ | See Fig. 7& 8 | ---- | 8.0 | 15 | | $T_J$ = 125°C | |
| $Q_{rr1}$ | Reverse Recovery Charge | ---- | 112 | 375 | nC | $T_J$ = 25°C | di/dt = 200A/µs |
| $Q_{rr2}$ | See Fig. 9 & 10 | ---- | 420 | 1200 | | $T_J$ = 125°C | |
| $di_{(rec)M}/dt1$ | Peak Rate of Fall of Recovery Current | ---- | 250 | ---- | A/µs | $T_J$ = 25°C | |
| $di_{(rec)M}/dt2$ | During $t_b$ See Fig. 11 & 12 | ---- | 160 | ---- | | $T_J$ = 125°C | |

## Thermal - Mechanical Characteristics

| | Parameter | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| $T_{lead}$① | Lead Temperature | ------ | ------ | 300 | °C |
| $R_{thJC}$ | Thermal Resistance, Junction to Case | ------ | ------ | 0.83 | K/W |
| $R_{thJA}$② | Thermal Resistance, Junction to Ambient | ------ | ------ | 40 | |
| $R_{thCS}$② | Thermal Resistance, Case to Heat Sink | ------ | 0.25 | ------ | |
| Wt | Weight | ------ | 6.0 | ------ | g |
| | | ------ | 0.21 | ------ | (oz) |
| | Mounting Torque | 6.0 | ------ | 12 | Kg-cm |
| | | 5.0 | ------ | 10 | lbf•in |

① 0.063 in. from Case (1.6mm) for 10 sec
② Typical Socket Mount
③ Mounting Surface, Flat, Smooth and Greased

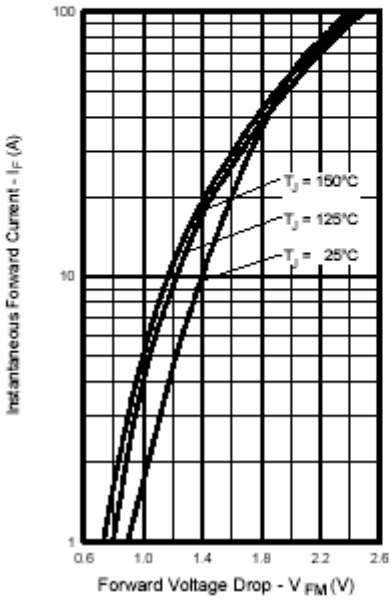



**Fig. 1** - Maximum Forward Voltage Drop vs. Instantaneous Forward Current

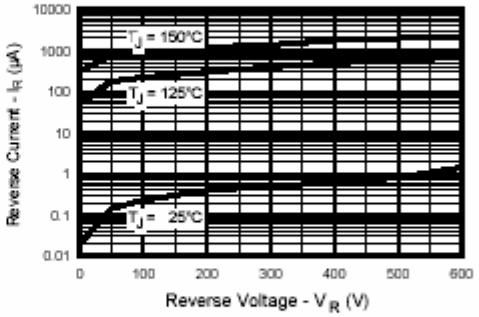



**Fig. 2** - Typical Reverse Current vs. Reverse Voltage

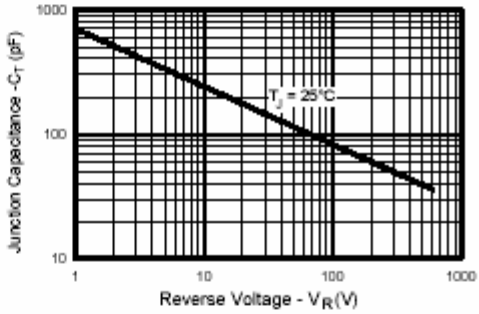



**Fig. 3** - Typical Junction Capacitance vs. Reverse Voltage

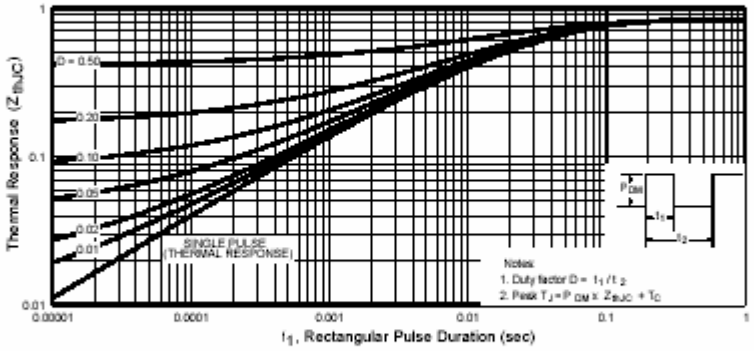



**Fig. 4** - Maximum Thermal Impedance $Z_{thjc}$ Characteristics

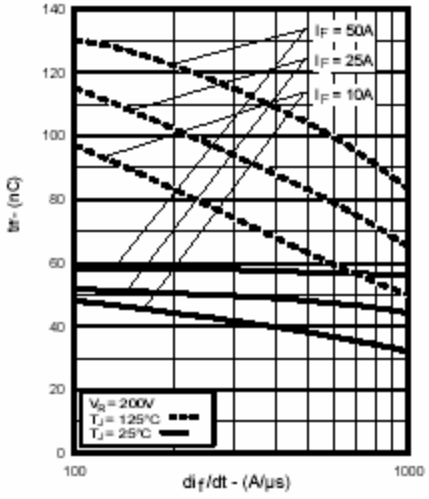



**Fig. 5** - Typical Reverse Recovery vs. $di_f/dt$

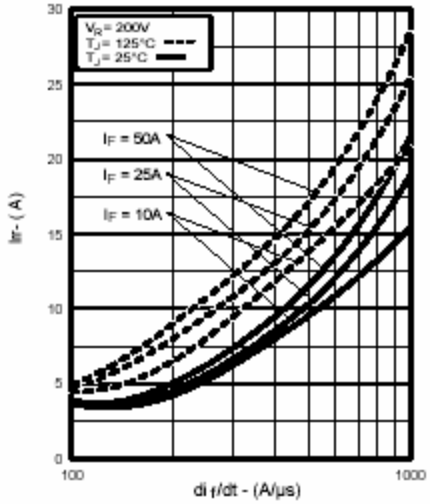



**Fig. 6** - Typical Recovery Current vs. $di_f/dt$

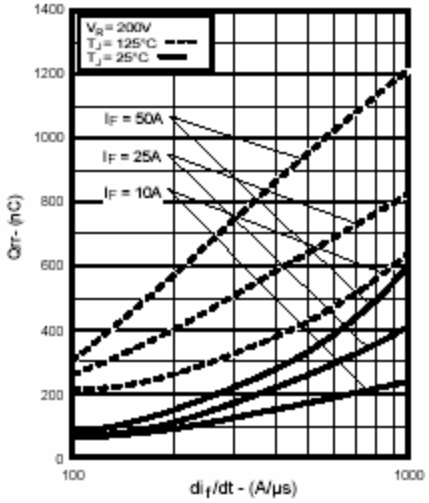



**Fig. 7** - Typical Stored Charge vs. $di_f/dt$

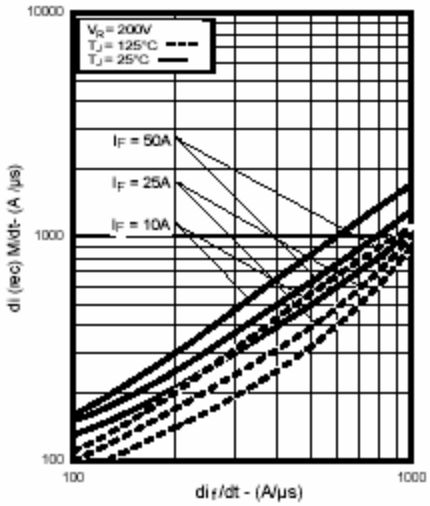



**Fig. 8** - Typical $di_{(rec)M}/dt$ vs. $di_f/dt$

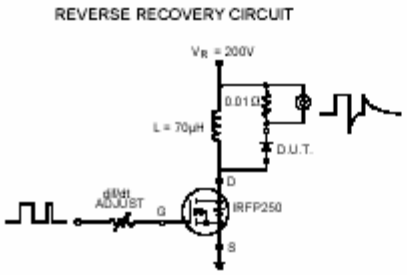
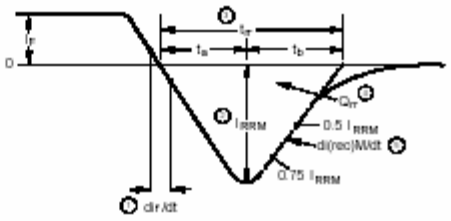



**Fig. 9** - Reverse Recovery Parameter Test Circuit

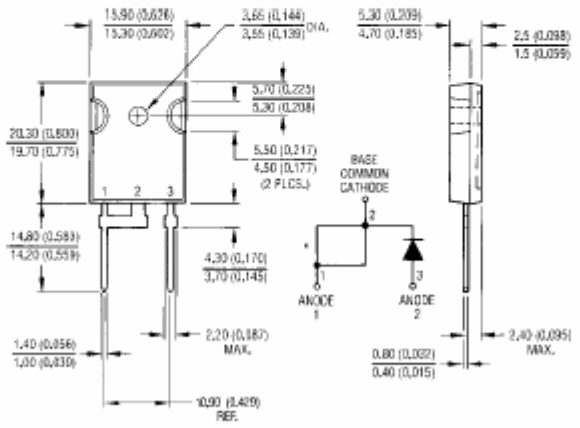



1. di/dt - Rate of change of current through zero crossing
2. $I_{RRM}$ - Peak reverse recovery current
3. trr - Reverse recovery time measured from zero crossing point of negative going IF to point where a line passing through 0.75 $I_{RRM}$ and 0.50 $I_{RRM}$ extrapolated to zero current
4. $Q_{rr}$ - Area under curve defined by $t_{rr}$ and $I_{RRM}$

$$Q_{rr} = \frac{t_{rr} \times I_{RRM}}{2}$$

5. $di_{(rec)M}/dt$ - Peak rate of change of current during $t_b$ portion of $t_{rr}$

**Fig. 10** - Reverse Recovery Waveform and Definitions

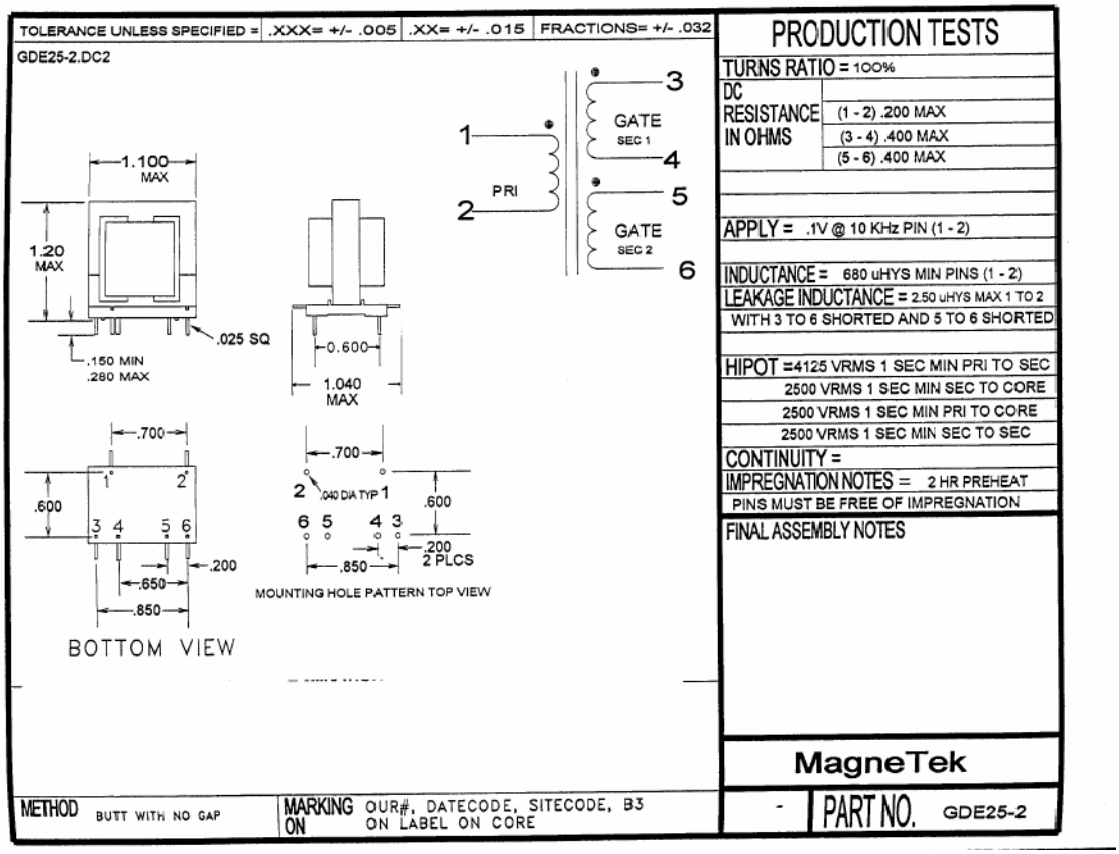



Conforms to JEDEC Outline TO-247AC MODIFIED
Dimensions in millimeters and inches

International
IOR Rectifier

**WORLD HEADQUARTERS:** 233 Kansas St., El Segundo, California 90245 U.S.A. Tel: (310) 322 3331. Fax: (310) 322 3332.
**EUROPEAN HEADQUARTERS:** Hurst Green, Oxted, Surrey RH8 9BB, U.K. Tel: ++ 44 1883 732020. Fax: ++ 44 1883 733408.
**IR CANADA:** 15 Lincoln Court, Brampton, Markham, Ontario L6T3Z2. Tel: (905) 453 2200. Fax: (905) 475 8801.
**IR GERMANY:** Saalburgstrasse 157, 61350 Bad Homburg. Tel: ++ 49 6172 96590. Fax: ++ 49 6172 965933.
**IR ITALY:** Via Liguria 49, 10071 Borgaro, Torino. Tel: ++ 39 11 4510111. Fax: ++ 39 11 4510220.
**IR FAR EAST:** K&H Bldg., 2F, 30-4 Nishi-Ikebukuro 3-Chome, Toshima-Ku, Tokyo, Japan 171. Tel: 81 3 3983 0086.
**IR SOUTHEAST ASIA:** 1 Kim Seng Promenade, Great World City West Tower, 13-11, Singapore 237994. Tel: ++ 65 838 4630.
**IR TAIWAN:** 16 Fl. Suite D.207, Sec. 2, Tun Haw South Road, Taipei, 10673, Taiwan. Tel: 886 2 2377 9936.

## D. SWITCHMODE/HIGH FREQUENCY GATE DRIVER TRANSFORMER [From Ref. 15.]



## E. TOSHIBA TLP250 OPTO-COUPLED GATE DRIVER [From Ref. 13.]

SEMICONDUCTOR
**TOSHIBA** TECHNICAL DATA

**TLP250**

(TLP250)
ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)

| | CHARACTERISTIC | | SYMBOL | RATING | UNIT |
|---|---|---|---|---|---|
| LED | Forward Current | | $I_F$ | 20 | mA |
| | Forward Current Derating (Ta ≧ 70°C) | | $\Delta I_F / \Delta Ta$ | −0.36 | mA / °C |
| | Peak Transient Forward Curent | (Note 1) | $I_{FPT}$ | 1 | A |
| | Reverse Voltage | | $V_R$ | 5 | V |
| | Junction Temperature | | $(T_j)$ | 125 | °C |
| DETECTOR | "H" Peak Output Current ($P_W \leqq 2.5\mu s$, f ≦ 15kHZ) | (Note 2) | $I_{OPH}$ | −1.5 | A |
| | "L" Peak Output Current ($P_W \leqq 2.5\mu s$, f ≦ 15kHZ) | (Note 2) | $I_{OPL}$ | +1.5 | A |
| | Output Voltage | (Ta ≦ 70°C) | $V_O$ | 35 | V |
| | | (Ta = 85°C) | | 24 | |
| | Supply Voltage | (Ta ≦ 70°C) | $V_{CC}$ | 35 | V |
| | | (Ta = 85°C) | | 24 | |
| | Output Voltage Derating (Ta ≧ 70°C) | | $\Delta V_O / \Delta Ta$ | −0.73 | V / °C |
| | Supply Voltage Derating (Ta ≧ 70°C) | | $\Delta V_{CC} / \Delta Ta$ | −0.73 | V / °C |
| | Junction Temperature | | $(T_j)$ | 125 | °C |
| Operating Frequency | | (Note 3) | f | 25 | kHz |
| Operating Temperature Range | | | $T_{opr}$ | −20~70 | °C |
| Storage Temperature Range | | | $T_{stg}$ | −55~125 | °C |
| Lead Solder Temperature (10s) | | | $T_{sol}$ | 260 | °C |
| Isolation Voltage (AC, 1min., R.H. ≦ 60%, Ta = 25°C) | | (Note 4) | $BV_S$ | 2500 | Vrms |

Note 1 : Pulse width $P_W \leqq 1\mu s$, 300pps

Note 2 : Exporenential Wavefom

Note 3 : Exporenential Wavefom, $I_{OPH} \leqq -1.0A$ ($\leqq 2.5\mu s$), $I_{OPL} \leqq +1.0A$ ($\leqq 2.5\mu s$)

Note 4 : Device considerd a two terminal device : pins 1,2,3 and 4 shorted together, and pins 5, 6, 7 and 8 shorted together.

Note 5 : A ceramic capacitor (0.1μF) should be connected from pin 8 to pin 5 to stabilize the operation of the high gain linear amplifier. Failure to provide the bypassing may impair the switching proparty. The total lead length between capacitor and coupler should not exceed 1cm.

RECOMMENDED OPERATING CONDITIONS

| CHARACTERISTIC | SYMBOL | MIN. | TYP. | MAX. | | UNIT |
|---|---|---|---|---|---|---|
| Input Current, ON | $I_{F(ON)}$ | 7 | 8 | 10 | | mA |
| Input Voltage, OFF | $V_{F(OFF)}$ | 0 | — | 0.8 | | V |
| Supply Voltage | $V_{CC}$ | 15 | — | 30 | 20 | V |
| Peak Output Current | $I_{OPH} / I_{OPL}$ | — | — | ±0.5 | | A |
| Operating Temperature | $T_{opr}$ | −20 | 25 | 70 | 85 | °C |

(TLP250)

ELECTRICAL CHARACTERISTICS (Ta = −20~70°C, Unless otherwise specified)

| CHARACTERISTIC | | SYMBOL | TEST CIR-CUIT | TEST CONDITION | | MIN. | TYP.* | MAX. | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| Input Forward Voltage | | $V_F$ | — | $I_F$=10mA, Ta=25°C | | | 1.6 | 1.8 | V |
| Temperature Coefficient of Forward Voltage | | $\Delta V_F / \Delta Ta$ | — | $I_F$=10mA | | — | −2.0 | — | mV/°C |
| Input Reverse Current | | $I_R$ | — | $V_R$=5V, Ta=25°C | | | — | 10 | μA |
| Input Capacitance | | $C_T$ | — | V=0, f=1MHz, Ta=25°C | | — | 45 | 250 | pF |
| Output Current | "H" Level | $I_{OPH}$ | 3 | $V_{CC}$=30V (*1) | $I_F$=10mA, $V_{8-6}$=4V | −0.5 | −1.5 | — | A |
| | "L" Level | $I_{OPL}$ | 2 | | $I_F$=0, $V_{6-5}$=9.5V | 0.5 | 2 | — | |
| Output Voltage | "H" Level | $V_{OH}$ | 4 | $V_{CC1}$=+15V, $V_{EE1}$=−15V, $R_L$=200Ω, $I_F$=5mA | | 11 | 12.8 | — | V |
| | "L" Level | $V_{OL}$ | 5 | $V_{CC1}$=+15V, $V_{EE1}$=−15V, $R_L$=200Ω, $V_F$=0.8V | | — | −14.2 | −12.5 | |
| Supply Current | "H" Level | $I_{CCH}$ | — | $V_{CC}$=30V, $I_F$=10mA, Ta=25°C | | — | 7 | — | mA |
| | | | | $V_{CC}$=30V, $I_F$=10mA | | — | — | 11 | |
| | "L" Level | $I_{CCL}$ | — | $V_{CC}$=30V, $I_F$=0mA, Ta=25°C | | — | 7.5 | — | |
| | | | | $V_{CC}$=30V, $I_F$=0mA | | — | — | 11 | |
| Threshold Input Current | "Output L→H" | $I_{FLH}$ | — | $V_{CC1}$=+15V, $V_{EE1}$=−15V, $R_L$=200Ω, $V_O$>0V | | — | 1.2 | 5 | mA |
| Threshold Input Voltage | "Output H→L" | $V_{FHL}$ | | $V_{CC1}$=+15V, $V_{EE1}$=−15V, $R_L$=200Ω, $V_O$<0V | | 0.8 | — | — | V |
| Supply Voltage | | $V_{CC}$ | — | | | 10 | — | 35 | V |
| Capacitance (Input-Output) | | $C_S$ | — | $V_S$=0, f=1MHz, Ta=25°C | | — | 1.0 | 2.0 | pF |
| Resistance (Input-Output) | | $R_S$ | — | $V_S$=500V, Ta=25°C, R.H.≤60% | | $5\times10^{10}$ | $10^{14}$ | — | Ω |

* All typical values are at Ta=25°C (*1) : Duration of $I_O$ time≤50μs

(TLP250)

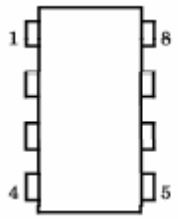
SWITCHING CHARACTERISTICS (Ta = −20~70°C, Unless otherwise specified)

| CHARACTERISTIC | | SYMBOL | TEST CIR-CUIT | TEST CONDITION | MIN. | TYP.* | MAX. | UNIT |
|---|---|---|---|---|---|---|---|---|
| Propagation Delay Time | L→H | $t_{pLH}$ | 6 | $I_F$ = 8mA | — | 0.15 | 0.5 | μs |
| | H→L | $t_{pHL}$ | | $V_{CC1}$ = +15V, $V_{EE1}$ = −15V | — | 0.15 | 0.5 | |
| Output Rise Time | | $t_r$ | | $R_L$ = 200Ω | — | | — | |
| Output Fall Time | | $t_f$ | | | — | | — | |
| Common Mode Transient Immunity at High Level Output | | $C_{MH}$ | 7 | $V_{CM}$ = 600V, $I_F$ = 8mA<br>$V_{CC}$ = 30V, Ta = 25°C | −5000 | — | — | V / μs |
| Common Mode Transient Immunity at Low Level Output | | $C_{ML}$ | 7 | $V_{CM}$ = 600V, $I_F$ = 0mA<br>$V_{CC}$ = 30V, Ta = 25°C | 5000 | — | — | V / μs |

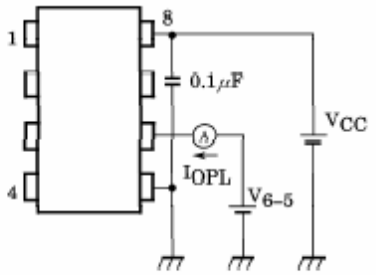
* All typical values are at Ta = 25°C

(TLP250)

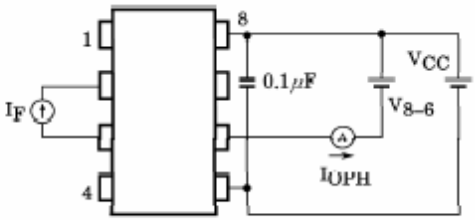
TEST CIRCUIT 1 :



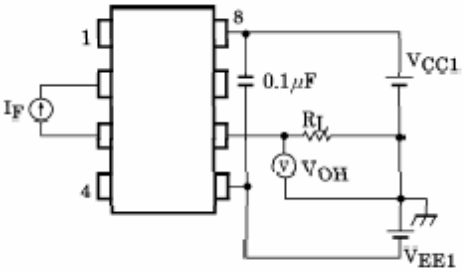

TEST CIRCUIT 2 : IOPL



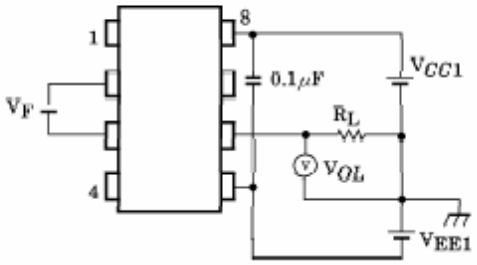

TEST CIRCUIT 3 : IOPH




TEST CIRCUIT 4 : VOH

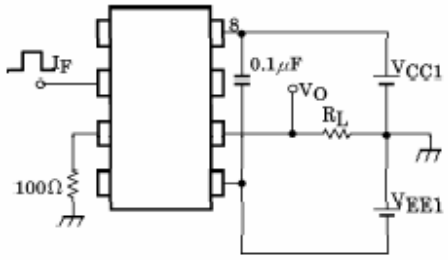


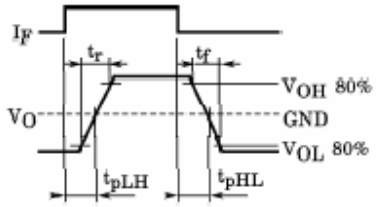

TEST CIRCUIT 5 : $V_{OL}$



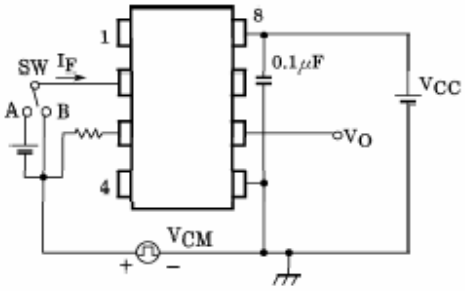
(TLP250)

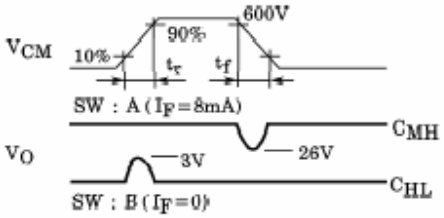
TEST CIRCUIT 6 : $t_{pLH}$, $t_{pHL}$, $t_r$, $t_f$




TEST CIRCUIT 7 : $C_{MH}$, $C_{ML}$



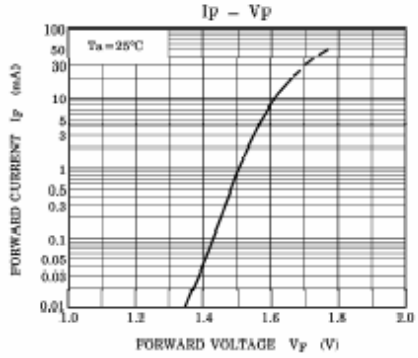

$$C_{ML} = \frac{480\,(V)}{t_r\,(\mu s)}$$

$$C_{MH} = \frac{480(V)}{t_f\,(\mu s)}$$

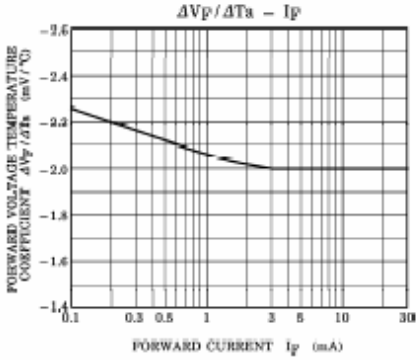
$C_{ML}$ ($C_{MH}$) is the maximum rate of rise (fall) of the common mode voltage that can be sustained with the output voltage in the low (high) state.

(TLP250)

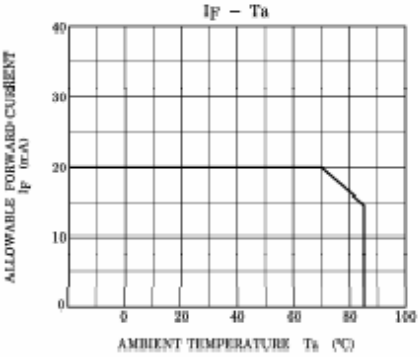
$I_P - V_P$



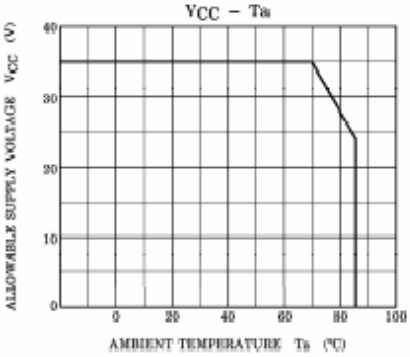

$\Delta V_F / \Delta Ta - I_F$



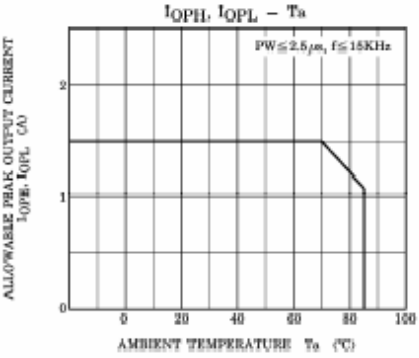

$I_F - Ta$




$V_{CC} - Ta$




$I_{OPH}, I_{OPL} - Ta$




TLP250 – 7*
1996 – 4 – 8
TOSHIBA CORPORATION

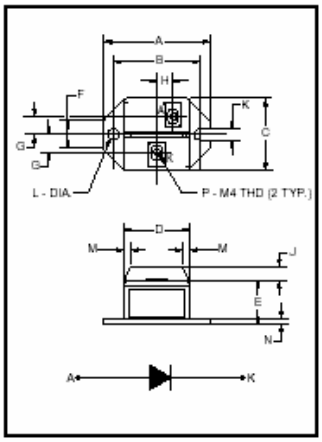
## F. POWEREX FAST RECOVERY SINGLE DIODE [From Ref. 16.]

POWEREX

*CS240650*
*CS241250*

*Powerex, Inc., 200 Hillis Street, Youngwood, Pennsylvania 15697-1800 (724) 925-7272*

***Fast Recovery Single Diode Modules***
***50 Amperes/600-1200 Volts***




Outline Drawing

| Dimension | Inches | Millimeters |
|---|---|---|
| A | 2.087 | 53 |
| B | 1.705±0.008 | 43.3±0.2 |
| C | 1.417 | 36 |
| D | 1.299 | 33 |
| E | 0.866 | 22 |
| F | 0.551 | 14 |
| G | 0.354 | 9 |
| H | 0.315 | 8 |
| J | 0.276 | 7 |
| K | 0.217 | 5.5 |
| L | 0.217 Dia. | Dia. 5.5 |
| M | 0.138 | 3.5 |
| N | 0.118 | 3 |
| P | M4 Metric | M4 |

CS240650, CS241250
Fast Recovery
Single Diode Modules
50 Amperes/600-1200 Volts

**Description:**
Powerex Fast Recovery Single Diode Modules are designed for use in applications requiring fast switching. The modules are isolated for easy mounting with other components on common heatsinks. POW-R-BLOK™ has been tested and recognized by Underwriters Laboratories (QQQX2 Power Switching Semiconductors).

**Features:**

- ☐ Isolated Mounting
- ☐ Planar Chips
- ☐ UL Recognized

**Applications:**

- ☐ Inverters
- ☐ Choppers
- ☐ Switching Power Supplies
- ☐ Free Wheeling

**Ordering Information:**
Select the complete eight digit module part number you desire from the table below.
Example: CS241250 is a 1200 Volt, 50 Ampere Fast Recovery Single Diode Module.

| Type | Voltage Volts (x100) | Current Rating Amperes (50) |
|---|---|---|
| CS24 | 06 | 50 |
| | 12 | |

D-9

Powerex, Inc., 200 Hillis Street, Youngwood, Pennsylvania 15697-1800 (724) 925-7272

*CS240650, CS241250*
*Fast Recovery Single Diode Modules*
*50 Amperes/600-1200 Volts*

**Absolute Maximum Ratings**

| Characteristics | Symbol | CS240650 | CS241250 | Units |
|---|---|---|---|---|
| Peak Reverse Blocking Voltage | $V_{RRM}$ | 600 | 1200 | Volts |
| Transient Peak Reverse Blocking Voltage (Non-Repetitive), t < 5ms | $V_{RSM}$ | 720 | 1350 | Volts |
| DC Reverse Blocking Voltage | $V_{R(DC)}$ | 480 | 960 | Volts |
| DC Current, $T_C$ = 105°C | $I_{F(DC)}$ | 50 | 50 | Amperes |
| Peak One-Cycle Surge (Non-Repetitive) On-State Current (60Hz) | $I_{FSM}$ | 1000 | 1000 | Amperes |
| Peak One-Cycle Surge (Non-Repetitive) On-State Current (50Hz) | $I_{FSM}$ | 910 | 910 | Amperes |
| I2t (for Fusing), 8.3 milliseconds | I2t | 4165 | 4165 | A2sec |
| Storage Temperature | $T_{STG}$ | -40 to 125 | -40 to 125 | °C |
| Operating Temperature | $T_j$ | -40 to 150 | -40 to 150 | °C |
| Maximum Mounting Torque M5 Mounting Screw | — | 17 | 17 | in.-lb. |
| Maximum Mounting Torque M4 Terminal Screw | — | 12 | 12 | in.-lb. |
| Module Weight (Typical) | — | 90 | 90 | Grams |
| V Isolation | $V_{RMS}$ | 2500 | 2500 | Volts |

*Powerex, Inc., 200 Hillis Street, Youngwood, Pennsylvania 15697-1800 (724) 925-7272*

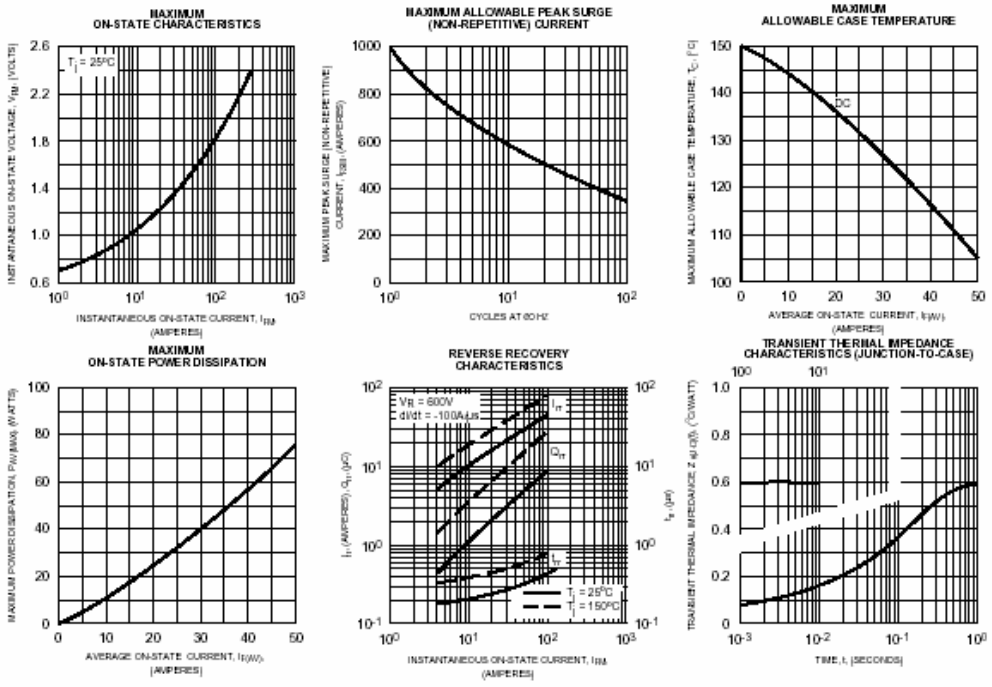
*CS240650, CS241250*
*Fast Recovery Single Diode Modules*
*50 Amperes/600-1200 Volts*

**Electrical and Thermal Characteristics, $T_j$ = 25°C unless otherwise specified**

| Characteristics | Symbol | Test Conditions | CS240650/CS241250 | Units |
|---|---|---|---|---|
| Blocking State Maximums | | | | |
| Reverse Leakage Current, Peak | $I_{RRM}$ | $T_j$ = 150°C, $V_{RRM}$ = Rated | 10 | mA |
| Conducting State Maximums | | | | |
| Peak On-State Voltage | $V_{FM}$ | $I_{FM}$ = 50A | 1.5 | Volts |
| Switching Minimums | | | | |
| Reverse Recovery Time | $t_{rr}$ | $I_{FM}$ = 50A, $T_j$ = 150°C<br>di/dt =-200A/µs, $V_R$ = 1/2 $V_{RRM}$ | 0.8 | µs |
| Reverse Recovery Charge | $Q_{rr}$ | $I_{FM}$ = 50A, $T_j$ = 150°C<br>di/dt =-200A/µs, $V_R$ = 1/2 $V_{RRM}$ | 30 | µC |
| Thermal Maximums | | | | |
| Thermal Resistance, Junction-to-Case | $R_{\theta(J-C)}$ | Per Module | 0.6 | °C/Watt |
| Thermal Resistance, Case-to-Sink (Lubricated) | $R_{\theta(C-S)}$ | Per Module | 0.4 | °C/Watt |

Powerex, Inc., 200 Hillis Street, Youngwood, Pennsylvania 15697-1800 (724) 925-7272

*CS240650, CS241250*
*Fast Recovery Single Diode Modules*
*50 Amperes/600-1200 Volts*



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# APENDIX B. MATLAB AND ABEL CODE

Appendix B contains written MATLAB code for the analysis of the power supply op-amp frequency response and it contains the ABEL code written for the programming of the digital logic controller devices.

## A. POWER SUPPLY OP-AMP FREQUENCY RESPONSE CODE

### 1. PowerSupplyOPAmp.m

```
% Power Supply 80W Op-Amp (LM12cl)
% This program is written to verify the frequency response of the
% LM12CL.

% ID Parts and their parameters

Rf = 3300; % Ohms
R1 = 1100; % Ohms
C1 = 1.5e-9; % Farads

% DC Gain of power supply

GainDC = 1 + (Rf/R1);

% AC Gain of power supply

num = [(Rf*R1*C1) (Rf+R1)];
den = [(Rf*R1*C1) (R1)];

TransFunc = TF(num,den)

bode(num,den)

SysPole = pole(TransFunc)
SysZero = zero(TransFunc)
```

## B. DIGITAL LOGIC CONTROL ABEL CODE

### 1. PwrFaze1.abl

```
MODULE PwrFaze1;
TITLE 'PwrFaze1'

DECLARATIONS

    PwrFaze1                 DEVICE  'P18CV8'               ;

"input pins
    A,B,C                   PIN     2,3,4                   ;
    D,E,F                   PIN     5,6,7                   ;

"output pins
    s,u,w,y                 PIN     12,14,16,18             ;
    s,u,w,y                 IsType  'com'                   ;

"equivalences

    Kntr        =           [A,B,C,D,E,F];      "set of inputs
    KnvrtrOut   =           [s,u,w,y];          "set of outputs
    H,L,X       =           1,0,.X.;            "rename constants
    ANYINPUT    =           [X,X,X,X,X,X];
    ANYOUTPUT   =           [X,X,X,X];

TRUTH_TABLE     ( [  Kntr  ] -> KnvrtrOut )
                  [    0   ] -> ^b0101 ;
                  [    1   ] -> ^b0101 ;
                  [    2   ] -> ^b0101 ;
                  [    3   ] -> ^b0101 ;
                  [    4   ] -> ^b0101 ;
                  [    5   ] -> ^b0101 ;
                  [    6   ] -> ^b0101 ;
                  [    7   ] -> ^b0101 ;
                  [    8   ] -> ^b0101 ;

                    [    9   ] ->   ^b0101 ; "5
                    [   10   ] ->   ^b0111 ; "7
                    [   11   ] ->   ^b0111 ; "7
                    [   12   ] ->   ^b0001 ; "1
                    [   13   ] ->   ^b0001 ; "1
                    [   14   ] ->   ^b0000 ; "0

                  [   15   ] -> ^b0101 ;
                  [   16   ] -> ^b0101 ;

                    [   17   ] ->   ^b0001 ; "1
                    [   18   ] ->   ^b0001 ; "1
                    [   19   ] ->   ^b0001 ; "1
                    [   20   ] ->   ^b0111 ; "7
                    [   21   ] ->   ^b0111 ; "7
                    [   22   ] ->   ^b0000 ; "0
```

```
[   23   ] -> ^b0101 ;
[   24   ] -> ^b0101 ;

  [   25   ] ->   ^b0001 ; "1
  [   26   ] ->   ^b0011 ; "3
  [   27   ] ->   ^b0011 ; "3
  [   28   ] ->   ^b0011 ; "3
  [   29   ] ->   ^b0011 ; "3
  [   30   ] ->   ^b0011 ; "3

[   31   ] -> ^b0101 ;
[   32   ] -> ^b0101 ;

  [   33   ] ->   ^b1101 ; "d
  [   34   ] ->   ^b1100 ; "c
  [   35   ] ->   ^b1100 ; "c
  [   36   ] ->   ^b1100 ; "c
  [   37   ] ->   ^b1100 ; "c
  [   38   ] ->   ^b1100 ; "c

[   39   ] -> ^b0101 ;
[   40   ] -> ^b0101 ;

  [   41   ] ->   ^b1101 ; "d
  [   42   ] ->   ^b1101 ; "d
  [   43   ] ->   ^b1101 ; "d
  [   44   ] ->   ^b0100 ; "4
  [   45   ] ->   ^b0100 ; "4
  [   46   ] ->   ^b1111 ; "f

[   47   ] -> ^b0101 ;
[   48   ] -> ^b0101 ;

  [   49   ] ->   ^b0101 ; "5
  [   50   ] ->   ^b0100 ; "4
  [   51   ] ->   ^b0100 ; "4
  [   52   ] ->   ^b1101 ; "d
  [   53   ] ->   ^b1101 ; "d
  [   54   ] ->   ^b1111 ; "f

[   55   ] -> ^b0101 ;
[   56   ] -> ^b0101 ;
[   57   ] -> ^b0101 ;
[   58   ] -> ^b0101 ;
[   59   ] -> ^b0101 ;
[   60   ] -> ^b0101 ;
[   61   ] -> ^b0101 ;
[   62   ] -> ^b0101 ;
[   63   ] -> ^b0101 ;
```

```
TEST_VECTORS    ( [ A,B,C,D,E,F ] -> [ s,u,w,y ] )

                  [ 0,0,0,0,0,0 ] -> [ 0, 1, 0, 1 ];
                  [ 0,0,0,0,0,1 ] -> [ 0, 1, 0, 1 ];
                  [ 0,0,0,0,1,0 ] -> [ 0, 1, 0, 1 ];
                  [ 0,0,0,0,1,1 ] -> [ 0, 1, 0, 1 ];
                  [ 0,0,0,1,0,0 ] -> [ 0, 1, 0, 1 ];
                  [ 0,0,0,1,0,1 ] -> [ 0, 1, 0, 1 ];
                  [ 0,0,0,1,1,0 ] -> [ 0, 1, 0, 1 ];
                  [ 0,0,0,1,1,1 ] -> [ 0, 1, 0, 1 ];
                  [ 0,0,1,0,0,0 ] -> [ 0, 1, 0, 1 ];

                      [ 0,0,1,0,0,1 ] -> [ 0, 1, 0, 1 ]; "5
                      [ 0,0,1,0,1,0 ] -> [ 0, 1, 1, 1 ]; "7
                      [ 0,0,1,0,1,1 ] -> [ 0, 1, 1, 1 ]; "7
                      [ 0,0,1,1,0,0 ] -> [ 0, 0, 0, 1 ]; "1
                      [ 0,0,1,1,0,1 ] -> [ 0, 0, 0, 1 ]; "1
                      [ 0,0,1,1,1,0 ] -> [ 0, 0, 0, 0 ]; "0

                  [ 0,0,1,1,1,1 ] -> [ 0, 1, 0, 1 ];
                  [ 0,1,0,0,0,0 ] -> [ 0, 1, 0, 1 ];

                      [ 0,1,0,0,0,1 ] -> [ 0, 0, 0, 1 ]; "1

                      [ 0,1,0,0,1,0 ] -> [ 0, 0, 0, 1 ]; "1
                      [ 0,1,0,0,1,1 ] -> [ 0, 0, 0, 1 ]; "1
                      [ 0,1,0,1,0,0 ] -> [ 0, 1, 1, 1 ]; "7
                      [ 0,1,0,1,0,1 ] -> [ 0, 1, 1, 1 ]; "7
                      [ 0,1,0,1,1,0 ] -> [ 0, 0, 0, 0 ]; "0

                  [ 0,1,0,1,1,1 ] -> [ 0, 1, 0, 1 ];
                  [ 0,1,1,0,0,0 ] -> [ 0, 1, 0, 1 ];

                      [ 0,1,1,0,0,1 ] -> [ 0, 0, 0, 1 ]; "1
                      [ 0,1,1,0,1,0 ] -> [ 0, 0, 1, 1 ]; "3
                      [ 0,1,1,0,1,1 ] -> [ 0, 0, 1, 1 ]; "3
                      [ 0,1,1,1,0,0 ] -> [ 0, 0, 1, 1 ]; "3
                      [ 0,1,1,1,0,1 ] -> [ 0, 0, 1, 1 ]; "3
                      [ 0,1,1,1,1,0 ] -> [ 0, 0, 1, 1 ]; "3

                  [ 0,1,1,1,1,1 ] -> [ 0, 1, 0, 1 ];
                  [ 1,0,0,0,0,0 ] -> [ 0, 1, 0, 1 ];

                      [ 1,0,0,0,0,1 ] -> [ 1, 1, 0, 1 ]; "d
                      [ 1,0,0,0,1,0 ] -> [ 1, 1, 0, 0 ]; "c
                      [ 1,0,0,0,1,1 ] -> [ 1, 1, 0, 0 ]; "c
                      [ 1,0,0,1,0,0 ] -> [ 1, 1, 0, 0 ]; "c
                      [ 1,0,0,1,0,1 ] -> [ 1, 1, 0, 0 ]; "c
                      [ 1,0,0,1,1,0 ] -> [ 1, 1, 0, 0 ]; "c

                  [ 1,0,0,1,1,1 ] -> [ 0, 1, 0, 1 ];
                  [ 1,0,1,0,0,0 ] -> [ 0, 1, 0, 1 ];
```

```
        [ 1,0,1,0,0,1 ] -> [ 1, 1, 0, 1 ]; "d
        [ 1,0,1,0,1,0 ] -> [ 1, 1, 0, 1 ]; "d
        [ 1,0,1,0,1,1 ] -> [ 1, 1, 0, 1 ]; "d
        [ 1,0,1,1,0,0 ] -> [ 0, 1, 0, 0 ]; "4
        [ 1,0,1,1,0,1 ] -> [ 0, 1, 0, 0 ]; "4
        [ 1,0,1,1,1,0 ] -> [ 1, 1, 1, 1 ]; "f

    [ 1,0,1,1,1,1 ] -> [ 0, 1, 0, 1 ];
    [ 1,1,0,0,0,0 ] -> [ 0, 1, 0, 1 ];

        [ 1,1,0,0,0,1 ] -> [ 0, 1, 0, 1 ]; "5
        [ 1,1,0,0,1,0 ] -> [ 0, 1, 0, 0 ]; "4
        [ 1,1,0,0,1,1 ] -> [ 0, 1, 0, 0 ]; "4
        [ 1,1,0,1,0,0 ] -> [ 1, 1, 0, 1 ]; "d
        [ 1,1,0,1,0,1 ] -> [ 1, 1, 0, 1 ]; "d
        [ 1,1,0,1,1,0 ] -> [ 1, 1, 1, 1 ]; "f

    [ 1,1,0,1,1,1 ] -> [ 0, 1, 0, 1 ];
    [ 1,1,1,0,0,0 ] -> [ 0, 1, 0, 1 ];
    [ 1,1,1,0,0,1 ] -> [ 0, 1, 0, 1 ];
    [ 1,1,1,0,1,0 ] -> [ 0, 1, 0, 1 ];
    [ 1,1,1,0,1,1 ] -> [ 0, 1, 0, 1 ];
    [ 1,1,1,1,0,0 ] -> [ 0, 1, 0, 1 ];
    [ 1,1,1,1,0,1 ] -> [ 0, 1, 0, 1 ];
    [ 1,1,1,1,1,0 ] -> [ 0, 1, 0, 1 ];
    [ 1,1,1,1,1,1 ] -> [ 0, 1, 0, 1 ];


END PwrFaze1
```

## 2. PwrFaze2.abl

```
MODULE PwrFaze2;
TITLE 'PwrFaze2'

DECLARATIONS

    PwrFaze2                DEVICE  'P18CV8'                ;

"input pins
    A,B,C                   PIN     2,3,4                    ;
    D,E,F                   PIN     5,6,7                    ;

"output pins
    s,u,w,y                 PIN     12,14,16,18              ;
    s,u,w,y                 IsType  'com'                    ;

"equivalences

    Kntr        =           [A,B,C,D,E,F];      "set of inputs
    KnvrtrOut   =           [s,u,w,y];          "set of outputs
    H,L,X       =           1,0,.X.;            "rename constants
    ANYINPUT    =           [X,X,X,X,X,X];
    ANYOUTPUT   =           [X,X,X,X];

TRUTH_TABLE     ( [  Kntr  ] -> KnvrtrOut )
                  [    0   ] -> ^b0101 ;
                  [    1   ] -> ^b0101 ;
                  [    2   ] -> ^b0101 ;
                  [    3   ] -> ^b0101 ;
                  [    4   ] -> ^b0101 ;
                  [    5   ] -> ^b0101 ;
                  [    6   ] -> ^b0101 ;
                  [    7   ] -> ^b0101 ;
                  [    8   ] -> ^b0101 ;

                    [    9   ] ->   ^b1101 ; "d
                    [   10   ] ->   ^b1100 ; "c
                    [   11   ] ->   ^b1100 ; "c
                    [   12   ] ->   ^b1100 ; "c
                    [   13   ] ->   ^b1100 ; "c
                    [   14   ] ->   ^b1100 ; "c

                  [   15   ] -> ^b0101 ;
                  [   16   ] -> ^b0101 ;

                    [   17   ] ->   ^b0101 ; "5
                    [   18   ] ->   ^b0111 ; "7
                    [   19   ] ->   ^b0111 ; "7
                    [   20   ] ->   ^b0001 ; "1
                    [   21   ] ->   ^b0001 ; "1
                    [   22   ] ->   ^b0000 ; "0

                  [   23   ] -> ^b0101 ;
                  [   24   ] -> ^b0101 ;
```

```
  [   25   ] ->   ^b1101 ; "d
  [   26   ] ->   ^b1101 ; "d
  [   27   ] ->   ^b1101 ; "d
  [   28   ] ->   ^b0100 ; "4
  [   29   ] ->   ^b0100 ; "4
  [   30   ] ->   ^b1111 ; "f

[   31   ] -> ^b0101 ;
[   32   ] -> ^b0101 ;

  [   33   ] ->   ^b0001 ; "1
  [   34   ] ->   ^b0001 ; "1
  [   35   ] ->   ^b0001 ; "1
  [   36   ] ->   ^b0111 ; "7
  [   37   ] ->   ^b0111 ; "7
  [   38   ] ->   ^b0000 ; "0

[   39   ] -> ^b0101 ;
[   40   ] -> ^b0101 ;

  [   41   ] ->   ^b0101 ; "5
  [   42   ] ->   ^b0100 ; "4
  [   43   ] ->   ^b0100 ; "4
  [   44   ] ->   ^b1101 ; "d
  [   45   ] ->   ^b1101 ; "d
  [   46   ] ->   ^b1111 ; "f

[   47   ] -> ^b0101 ;
[   48   ] -> ^b0101 ;

  [   49   ] ->   ^b0001 ; "1
  [   50   ] ->   ^b0011 ; "3
  [   51   ] ->   ^b0011 ; "3
  [   52   ] ->   ^b0011 ; "3
  [   53   ] ->   ^b0011 ; "3
  [   54   ] ->   ^b0011 ; "3

[   55   ] -> ^b0101 ;
[   56   ] -> ^b0101 ;
[   57   ] -> ^b0101 ;
[   58   ] -> ^b0101 ;
[   59   ] -> ^b0101 ;
[   60   ] -> ^b0101 ;
[   61   ] -> ^b0101 ;
[   62   ] -> ^b0101 ;
[   63   ] -> ^b0101 ;
```

```
TEST_VECTORS    ( [ A,B,C,D,E,F ] -> [ s,u,w,y ] )

                  [ 0,0,0,0,0,0 ] -> [ 0, 1, 0, 1 ];
                  [ 0,0,0,0,0,1 ] -> [ 0, 1, 0, 1 ];
                  [ 0,0,0,0,1,0 ] -> [ 0, 1, 0, 1 ];
                  [ 0,0,0,0,1,1 ] -> [ 0, 1, 0, 1 ];
                  [ 0,0,0,1,0,0 ] -> [ 0, 1, 0, 1 ];
                  [ 0,0,0,1,0,1 ] -> [ 0, 1, 0, 1 ];
                  [ 0,0,0,1,1,0 ] -> [ 0, 1, 0, 1 ];
                  [ 0,0,0,1,1,1 ] -> [ 0, 1, 0, 1 ];
                  [ 0,0,1,0,0,0 ] -> [ 0, 1, 0, 1 ];

                      [ 0,0,1,0,0,1 ] -> [ 1, 1, 0, 1 ]; "d
                      [ 0,0,1,0,1,0 ] -> [ 1, 1, 0, 0 ]; "c
                      [ 0,0,1,0,1,1 ] -> [ 1, 1, 0, 0 ]; "c
                      [ 0,0,1,1,0,0 ] -> [ 1, 1, 0, 0 ]; "c
                      [ 0,0,1,1,0,1 ] -> [ 1, 1, 0, 0 ]; "c
                      [ 0,0,1,1,1,0 ] -> [ 1, 1, 0, 0 ]; "c

                  [ 0,0,1,1,1,1 ] -> [ 0, 1, 0, 1 ];
                  [ 0,1,0,0,0,0 ] -> [ 0, 1, 0, 1 ];

                      [ 0,1,0,0,0,1 ] -> [ 0, 1, 0, 1 ]; "5
                      [ 0,1,0,0,1,0 ] -> [ 0, 1, 1, 1 ]; "7
                      [ 0,1,0,0,1,1 ] -> [ 0, 1, 1, 1 ]; "7
                      [ 0,1,0,1,0,0 ] -> [ 0, 0, 0, 1 ]; "1
                      [ 0,1,0,1,0,1 ] -> [ 0, 0, 0, 1 ]; "1
                      [ 0,1,0,1,1,0 ] -> [ 0, 0, 0, 0 ]; "0

                  [ 0,1,0,1,1,1 ] -> [ 0, 1, 0, 1 ];
                  [ 0,1,1,0,0,0 ] -> [ 0, 1, 0, 1 ];

                      [ 0,1,1,0,0,1 ] -> [ 1, 1, 0, 1 ]; "d
                      [ 0,1,1,0,1,0 ] -> [ 1, 1, 0, 1 ]; "d
                      [ 0,1,1,0,1,1 ] -> [ 1, 1, 0, 1 ]; "d
                      [ 0,1,1,1,0,0 ] -> [ 0, 1, 0, 0 ]; "4
                      [ 0,1,1,1,0,1 ] -> [ 0, 1, 0, 0 ]; "4
                      [ 0,1,1,1,1,0 ] -> [ 1, 1, 1, 1 ]; "f

                  [ 0,1,1,1,1,1 ] -> [ 0, 1, 0, 1 ];
                  [ 1,0,0,0,0,0 ] -> [ 0, 1, 0, 1 ];

                      [ 1,0,0,0,0,1 ] -> [ 0, 0, 0, 1 ]; "1
                      [ 1,0,0,0,1,0 ] -> [ 0, 0, 0, 1 ]; "1
                      [ 1,0,0,0,1,1 ] -> [ 0, 0, 0, 1 ]; "1
                      [ 1,0,0,1,0,0 ] -> [ 0, 1, 1, 1 ]; "7
                      [ 1,0,0,1,0,1 ] -> [ 0, 1, 1, 1 ]; "7
                      [ 1,0,0,1,1,0 ] -> [ 0, 0, 0, 0 ]; "0

                  [ 1,0,0,1,1,1 ] -> [ 0, 1, 0, 1 ];
                  [ 1,0,1,0,0,0 ] -> [ 0, 1, 0, 1 ];
```

```
        [ 1,0,1,0,0,1 ] -> [ 0, 1, 0, 1 ]; "5
        [ 1,0,1,0,1,0 ] -> [ 0, 1, 0, 0 ]; "4
        [ 1,0,1,0,1,1 ] -> [ 0, 1, 0, 0 ]; "4
        [ 1,0,1,1,0,0 ] -> [ 1, 1, 0, 1 ]; "d
        [ 1,0,1,1,0,1 ] -> [ 1, 1, 0, 1 ]; "d
        [ 1,0,1,1,1,0 ] -> [ 1, 1, 1, 1 ]; "f

    [ 1,0,1,1,1,1 ] -> [ 0, 1, 0, 1 ];
    [ 1,1,0,0,0,0 ] -> [ 0, 1, 0, 1 ];

        [ 1,1,0,0,0,1 ] -> [ 0, 0, 0, 1 ]; "1
        [ 1,1,0,0,1,0 ] -> [ 0, 0, 1, 1 ]; "3
        [ 1,1,0,0,1,1 ] -> [ 0, 0, 1, 1 ]; "3
        [ 1,1,0,1,0,0 ] -> [ 0, 0, 1, 1 ]; "3
        [ 1,1,0,1,0,1 ] -> [ 0, 0, 1, 1 ]; "3
        [ 1,1,0,1,1,0 ] -> [ 0, 0, 1, 1 ]; "3

    [ 1,1,0,1,1,1 ] -> [ 0, 1, 0, 1 ];
    [ 1,1,1,0,0,0 ] -> [ 0, 1, 0, 1 ];
    [ 1,1,1,0,0,1 ] -> [ 0, 1, 0, 1 ];
    [ 1,1,1,0,1,0 ] -> [ 0, 1, 0, 1 ];
    [ 1,1,1,0,1,1 ] -> [ 0, 1, 0, 1 ];
    [ 1,1,1,1,0,0 ] -> [ 0, 1, 0, 1 ];
    [ 1,1,1,1,0,1 ] -> [ 0, 1, 0, 1 ];
    [ 1,1,1,1,1,0 ] -> [ 0, 1, 0, 1 ];
    [ 1,1,1,1,1,1 ] -> [ 0, 1, 0, 1 ];


END PwrFaze2
```

### 3. PwrFaze3.abl

```
MODULE PwrFaze3;
TITLE 'PwrFaze3'

DECLARATIONS

    PwrFaze3                DEVICE  'P18CV8'                ;

"input pins
    A,B,C                   PIN     2,3,4                   ;
    D,E,F                   PIN     5,6,7                   ;

"output pins
    s,u,w,y                 PIN     12,14,16,18             ;
    s,u,w,y                 IsType  'com'                   ;

"equivalences

    Kntr        =           [A,B,C,D,E,F];      "set of inputs
    KnvrtrOut   =           [s,u,w,y];          "set of outputs
    H,L,X       =           1,0,.X.;            "rename constants
    ANYINPUT    =           [X,X,X,X,X,X];
    ANYOUTPUT   =           [X,X,X,X];

TRUTH_TABLE     ( [  Kntr  ] -> KnvrtrOut )
                  [    0   ] -> ^b0101 ;
                  [    1   ] -> ^b0101 ;
                  [    2   ] -> ^b0101 ;
                  [    3   ] -> ^b0101 ;
                  [    4   ] -> ^b0101 ;
                  [    5   ] -> ^b0101 ;
                  [    6   ] -> ^b0101 ;
                  [    7   ] -> ^b0101 ;
                  [    8   ] -> ^b0101 ;

                    [    9   ] ->   ^b0001 ; "1
                    [   10   ] ->   ^b0001 ; "1
                    [   11   ] ->   ^b0001 ; "1
                    [   12   ] ->   ^b0111 ; "7
                    [   13   ] ->   ^b0111 ; "7
                    [   14   ] ->   ^b0000 ; "0

                  [   15   ] -> ^b0101 ;
                  [   16   ] -> ^b0101 ;

                    [   17   ] ->   ^b1101 ; "d
                    [   18   ] ->   ^b1100 ; "c
                    [   19   ] ->   ^b1100 ; "c
                    [   20   ] ->   ^b1100 ; "c
                    [   21   ] ->   ^b1100 ; "c
                    [   22   ] ->   ^b1100 ; "c

                  [   23   ] -> ^b0101 ;
                  [   24   ] -> ^b0101 ;
```

```
  [   25   ] ->   ^b0101 ; "5
  [   26   ] ->   ^b0100 ; "4
  [   27   ] ->   ^b0100 ; "4
  [   28   ] ->   ^b1101 ; "d
  [   29   ] ->   ^b1101 ; "d
  [   30   ] ->   ^b1111 ; "f

[   31   ] -> ^b0101 ;
[   32   ] -> ^b0101 ;

  [   33   ] ->   ^b0101 ; "5
  [   34   ] ->   ^b0111 ; "7
  [   35   ] ->   ^b0111 ; "7
  [   36   ] ->   ^b0001 ; "1
  [   37   ] ->   ^b0001 ; "1
  [   38   ] ->   ^b0000 ; "0

[   39   ] -> ^b0101 ;
[   40   ] -> ^b0101 ;

  [   41   ] ->   ^b0001 ; "1
  [   42   ] ->   ^b0011 ; "3
  [   43   ] ->   ^b0011 ; "3
  [   44   ] ->   ^b0011 ; "3
  [   45   ] ->   ^b0011 ; "3
  [   46   ] ->   ^b0011 ; "3

[   47   ] -> ^b0101 ;
[   48   ] -> ^b0101 ;

  [   49   ] ->   ^b1101 ; "d
  [   50   ] ->   ^b1101 ; "d
  [   51   ] ->   ^b1101 ; "d
  [   52   ] ->   ^b0100 ; "4
  [   53   ] ->   ^b0100 ; "4
  [   54   ] ->   ^b1111 ; "f

[   55   ] -> ^b0101 ;
[   56   ] -> ^b0101 ;
[   57   ] -> ^b0101 ;
[   58   ] -> ^b0101 ;
[   59   ] -> ^b0101 ;
[   60   ] -> ^b0101 ;
[   61   ] -> ^b0101 ;
[   62   ] -> ^b0101 ;
[   63   ] -> ^b0101 ;
```

```
TEST_VECTORS    ( [ A,B,C,D,E,F ] -> [ s,u,w,y ] )

                  [ 0,0,0,0,0,0 ] -> [ 0, 1, 0, 1 ];
                  [ 0,0,0,0,0,1 ] -> [ 0, 1, 0, 1 ];
                  [ 0,0,0,0,1,0 ] -> [ 0, 1, 0, 1 ];
                  [ 0,0,0,0,1,1 ] -> [ 0, 1, 0, 1 ];
                  [ 0,0,0,1,0,0 ] -> [ 0, 1, 0, 1 ];
                  [ 0,0,0,1,0,1 ] -> [ 0, 1, 0, 1 ];
                  [ 0,0,0,1,1,0 ] -> [ 0, 1, 0, 1 ];
                  [ 0,0,0,1,1,1 ] -> [ 0, 1, 0, 1 ];
                  [ 0,0,1,0,0,0 ] -> [ 0, 1, 0, 1 ];

                      [ 0,0,1,0,0,1 ] -> [ 0, 0, 0, 1 ]; "1
                      [ 0,0,1,0,1,0 ] -> [ 0, 0, 0, 1 ]; "1
                      [ 0,0,1,0,1,1 ] -> [ 0, 0, 0, 1 ]; "1
                      [ 0,0,1,1,0,0 ] -> [ 0, 1, 1, 1 ]; "7
                      [ 0,0,1,1,0,1 ] -> [ 0, 1, 1, 1 ]; "7
                      [ 0,0,1,1,1,0 ] -> [ 0, 0, 0, 0 ]; "0

                  [ 0,0,1,1,1,1 ] -> [ 0, 1, 0, 1 ];
                  [ 0,1,0,0,0,0 ] -> [ 0, 1, 0, 1 ];

                      [ 0,1,0,0,0,1 ] -> [ 1, 1, 0, 1 ]; "d
                      [ 0,1,0,0,1,0 ] -> [ 1, 1, 0, 0 ]; "c
                      [ 0,1,0,0,1,1 ] -> [ 1, 1, 0, 0 ]; "c
                      [ 0,1,0,1,0,0 ] -> [ 1, 1, 0, 0 ]; "c
                      [ 0,1,0,1,0,1 ] -> [ 1, 1, 0, 0 ]; "c
                      [ 0,1,0,1,1,0 ] -> [ 1, 1, 0, 0 ]; "c

                  [ 0,1,0,1,1,1 ] -> [ 0, 1, 0, 1 ];
                  [ 0,1,1,0,0,0 ] -> [ 0, 1, 0, 1 ];

                      [ 0,1,1,0,0,1 ] -> [ 0, 1, 0, 1 ]; "5
                      [ 0,1,1,0,1,0 ] -> [ 0, 1, 0, 0 ]; "4
                      [ 0,1,1,0,1,1 ] -> [ 0, 1, 0, 0 ]; "4
                      [ 0,1,1,1,0,0 ] -> [ 1, 1, 0, 1 ]; "d
                      [ 0,1,1,1,0,1 ] -> [ 1, 1, 0, 1 ]; "d
                      [ 0,1,1,1,1,0 ] -> [ 1, 1, 1, 1 ]; "f

                  [ 0,1,1,1,1,1 ] -> [ 0, 1, 0, 1 ];
                  [ 1,0,0,0,0,0 ] -> [ 0, 1, 0, 1 ];

                      [ 1,0,0,0,0,1 ] -> [ 0, 1, 0, 1 ]; "5
                      [ 1,0,0,0,1,0 ] -> [ 0, 1, 1, 1 ]; "7
                      [ 1,0,0,0,1,1 ] -> [ 0, 1, 1, 1 ]; "7
                      [ 1,0,0,1,0,0 ] -> [ 0, 0, 0, 1 ]; "1
                      [ 1,0,0,1,0,1 ] -> [ 0, 0, 0, 1 ]; "1
                      [ 1,0,0,1,1,0 ] -> [ 0, 0, 0, 0 ]; "0

                  [ 1,0,0,1,1,1 ] -> [ 0, 1, 0, 1 ];
                  [ 1,0,1,0,0,0 ] -> [ 0, 1, 0, 1 ];

                      [ 1,0,1,0,0,1 ] -> [ 0, 0, 0, 1 ]; "1
                      [ 1,0,1,0,1,0 ] -> [ 0, 0, 1, 1 ]; "3
                      [ 1,0,1,0,1,1 ] -> [ 0, 0, 1, 1 ]; "3
```

```
        [ 1,0,1,1,0,0 ] -> [ 0, 0, 1, 1 ]; "3
        [ 1,0,1,1,0,1 ] -> [ 0, 0, 1, 1 ]; "3
        [ 1,0,1,1,1,0 ] -> [ 0, 0, 1, 1 ]; "3

    [ 1,0,1,1,1,1 ] -> [ 0, 1, 0, 1 ];
    [ 1,1,0,0,0,0 ] -> [ 0, 1, 0, 1 ];

        [ 1,1,0,0,0,1 ] -> [ 1, 1, 0, 1 ]; "d
        [ 1,1,0,0,1,0 ] -> [ 1, 1, 0, 1 ]; "d
        [ 1,1,0,0,1,1 ] -> [ 1, 1, 0, 1 ]; "d
        [ 1,1,0,1,0,0 ] -> [ 0, 1, 0, 0 ]; "4
        [ 1,1,0,1,0,1 ] -> [ 0, 1, 0, 0 ]; "4
        [ 1,1,0,1,1,0 ] -> [ 1, 1, 1, 1 ]; "f

    [ 1,1,0,1,1,1 ] -> [ 0, 1, 0, 1 ];
    [ 1,1,1,0,0,0 ] -> [ 0, 1, 0, 1 ];
    [ 1,1,1,0,0,1 ] -> [ 0, 1, 0, 1 ];
    [ 1,1,1,0,1,0 ] -> [ 0, 1, 0, 1 ];
    [ 1,1,1,0,1,1 ] -> [ 0, 1, 0, 1 ];
    [ 1,1,1,1,0,0 ] -> [ 0, 1, 0, 1 ];
    [ 1,1,1,1,0,1 ] -> [ 0, 1, 0, 1 ];
    [ 1,1,1,1,1,0 ] -> [ 0, 1, 0, 1 ];
    [ 1,1,1,1,1,1 ] -> [ 0, 1, 0, 1 ];


END PwrFaze3
```

### 4. MOD6KNTR.ABL

```
MODULE MOD6KNTR                                                    ;

TITLE 'MOD6KNTR'

DECLARATIONS

    MOD6KNTR                DEVICE  'P18CV8'                       ;

"input pins
    CLOCK,COUNT             PIN     1,2                            ;

    " output pins

    x0,y0,z0,x1,y1,z1       PIN     19,18,17,16,15,14              ;
    x0,y0,z0,x1,y1,z1       IsType  'feed_reg,reg_d,pos'           ;

EQUATIONS
    x1 := !COUNT&x1 # COUNT&!z1&(x1#y1)                             ;
    y1 := !COUNT&y1 # COUNT&!x1                                     ;
    z1 := !COUNT&z1 # COUNT&!y1                                     ;
    x0 := x0&(!COUNT#!(x1&!y1&z1)) # !z0&COUNT&(x1&!y1&z1)&(x0#y0)  ;
    y0 := y0&(!COUNT#!(x1&!y1&z1)) # !x0&COUNT&(x1&!y1&z1)          ;
    z0 := z0&(!COUNT#!(x1&!y1&z1)) # !y0&COUNT&(x1&!y1&z1)          ;

TEST_VECTORS    ( [ CLOCK,COUNT ] -> [ x0,y0,z0,x1,y1,z1 ] )
                  [  .C. ,  1   ] -> [  0, 0, 0, 0, 1, 1 ]          ;
                  [  .C. ,  1   ] -> [  0, 0, 0, 0, 1, 0 ]          ;
                  [  .C. ,  1   ] -> [  0, 0, 0, 1, 1, 0 ]          ;
                  [  .C. ,  1   ] -> [  0, 0, 0, 1, 0, 0 ]          ;
                  [  .C. ,  1   ] -> [  0, 0, 0, 1, 0, 1 ]          ;

                  [  .C. ,  1   ] -> [  0, 1, 1, 0, 0, 1 ]          ;
                  [  .C. ,  1   ] -> [  0, 1, 1, 0, 1, 1 ]          ;
                  [  .C. ,  1   ] -> [  0, 1, 1, 0, 1, 0 ]          ;
                  [  .C. ,  1   ] -> [  0, 1, 1, 1, 1, 0 ]          ;
                  [  .C. ,  1   ] -> [  0, 1, 1, 1, 0, 0 ]          ;
                  [  .C. ,  1   ] -> [  0, 1, 1, 1, 0, 1 ]          ;

                  [  .C. ,  1   ] -> [  0, 1, 0, 0, 0, 1 ]          ;
                  [  .C. ,  1   ] -> [  0, 1, 0, 0, 1, 1 ]          ;
                  [  .C. ,  1   ] -> [  0, 1, 0, 0, 1, 0 ]          ;
                  [  .C. ,  1   ] -> [  0, 1, 0, 1, 1, 0 ]          ;
                  [  .C. ,  1   ] -> [  0, 1, 0, 1, 0, 0 ]          ;
                  [  .C. ,  1   ] -> [  0, 1, 0, 1, 0, 1 ]          ;

                  [  .C. ,  1   ] -> [  1, 1, 0, 0, 0, 1 ]          ;
                  [  .C. ,  1   ] -> [  1, 1, 0, 0, 1, 1 ]          ;
                  [  .C. ,  1   ] -> [  1, 1, 0, 0, 1, 0 ]          ;
                  [  .C. ,  1   ] -> [  1, 1, 0, 1, 1, 0 ]          ;
                  [  .C. ,  1   ] -> [  1, 1, 0, 1, 0, 0 ]          ;
                  [  .C. ,  1   ] -> [  1, 1, 0, 1, 0, 1 ]          ;

                  [  .C. ,  1   ] -> [  1, 0, 0, 0, 0, 1 ]          ;
```

```
                    [  .C. ,  1   ] -> [  1, 0, 0, 0, 1, 1 ]          ;
                    [  .C. ,  1   ] -> [  1, 0, 0, 0, 1, 0 ]          ;
                    [  .C. ,  1   ] -> [  1, 0, 0, 1, 1, 0 ]          ;
                    [  .C. ,  1   ] -> [  1, 0, 0, 1, 0, 0 ]          ;
                    [  .C. ,  1   ] -> [  1, 0, 0, 1, 0, 1 ]          ;

                    [  .C. ,  1   ] -> [  1, 0, 1, 0, 0, 1 ]          ;
                    [  .C. ,  1   ] -> [  1, 0, 1, 0, 1, 1 ]          ;
                    [  .C. ,  1   ] -> [  1, 0, 1, 0, 1, 0 ]          ;
                    [  .C. ,  1   ] -> [  1, 0, 1, 1, 1, 0 ]          ;
                    [  .C. ,  1   ] -> [  1, 0, 1, 1, 0, 0 ]          ;
                    [  .C. ,  1   ] -> [  1, 0, 1, 1, 0, 1 ]          ;

                    [  .C. ,  1   ] -> [  0, 0, 1, 0, 0, 1 ]          ;
                    [  .C. ,  1   ] -> [  0, 0, 1, 0, 1, 1 ]          ;

END MOD6KNTR
```

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## APENDIX C. PARTS LIST

Appendix C contains the part lists for the Power Supply Op-Amp circuit, Gate-Driver circuit, the IGBT and Snubber circuit and for the power unit and converter.

### A. POWER SUPPLY OP-AMP CIRCUIT PARTS LIST

| Part Name | Part Number | Value | Qty |
|---|---|---|---|
| Operational Amplifier | LM12CL | 80 kW | 1 |
| Resistor | -- | 1.1 kΩ | 1 |
| Resistor | -- | 3.3 kΩ | 1 |
| Resistor | -- | 50 Ω | 1 |
| Resistor | -- | 2.2 Ω | 1 |
| Capacitor | P6710 | 2200 µF | 2 |
| Capacitor | -- | 1.5 nF | 1 |
| Diode | UF1003 | -- | 2 |
| Heat Sink | Type 341K | -- | 2 |
| Connector, Banana Plug | -- | -- | 2 |
| Connector, BNC | -- | -- | 2 |

### B. GATE DRIVER CIRCUIT CARD PARTS LIST

| Part Name | Part Number | Value | Qty |
|---|---|---|---|
| 8-Dip PhotoCoupler IGBT | TLP250-ND | -- | 1 |
| Gate Driver Transformer | GDE 25-2 | 0.650 Ω | 1 |
| Diode, Rectifier | 1N4148MSCT | 0.15 A | 6 |
| Capacitor | P4966 | 1.0 µF | 1 |
| Capacitor | -- | 1.0 µF | 4 |
| Resistor | -- | 360 Ω | 1 |
| Resistor | -- | 5 Ω | 1 |
| Connector, BNC | -- | -- | 1 |
| Connector, 2 Slot | -- | -- | 1 |

### C. IGBT AND SNUBBER CIRCUIT CARD PARTS LIST

| Part Name | Part Number | Value | Qty |
|---|---|---|---|
| IGBT | IRG4PH50KD | 25 A | 1 |
| Diode, HEXFRED | HFA25PB60 | 25 A | 1 |
| Resistor | TBH25P10R0J | 10 Ω | 1 |
| Capacitor | P3512 | 0.018 µF | 1 |
| Diode, Zener | 1N4744DICT | 15V | 2 |
| Connector, 3 Slot | -- | -- | 1 |
| Connector, 2 Slot | -- | -- | 1 |
| Heat Sink, Aluminum Strip | -- | -- | 2 |

## D. POWER UNIT PARTS LIST

| Part Name/Component | Part Number | Value | Qty |
|---|---|---|---|
| Gate Driver Circuit Card | -- | -- | 1 |
| IGBT/Snubber Circuit Card | -- | -- | 1 |
| Posts, Metal | -- | -- | 2 |
| Heat Sink | Type 641K | -- | 1 |

## E. CONVERTER PARTS LIST (ONE PHASE)

| Part Name/Component | Part Number | Value | Qty |
|---|---|---|---|
| Power Unit | -- | -- | 8 |
| Capacitor | CGH102T450V3L | 1000 µF | 4 |
| Power Diode | PRX-N16AA2 | -- | 4 |
| Capacitor | -- | 22 µF | 4 |
| Conduit, Copper | -- | cm | 24 |

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